Commercial AIO Chassis System

Project name: Woody
SCH Ver: SA
PCB Number: 15033-SA

PAGE	TITLE	Quantity
01	COVER PAGE	
02	BLOCK DIAGRAM	
03	CPU (PCIE/DMI)	
04	CPU_(THERMAL/CLOCK/PM/CFG)	
05	CPU_(DDR4 CHANNEL A)	
06	CPU_(DDR4 CHANNEL B)	
07	CPU (DDI/EDP)	
08	CPU (CPU Power)	
09	CPU (VSS)	
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11	DDR4 DIMM_1	
12	DDR4 DIMM_2	
13	DDR4 DIMM_3_(R)	
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15	PCH (SPI/UART/I2C)	
16	PCH (DMI/PCI-E/USB)DDI GP	
17	PCH (PCI-E/SATA)	
18	PCH (CLOCK/CL)	
19	PCH (USB/ESPI)	
20	PCH(GPIO/CPU/SMBUS/IHDA/JTAG)	
21	PCH (POWER1)	
22	PCH (POWER2)_PCH Strap	
23	PCH Power CAP	
24	SIO ITE8732F_CX	
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26	Thermal&FAN	
27	Audio Codec_ALC269	
28	Audio_AMP	
29	Audio IO_Combo HP_MIC	
30	Audio IO_Side	
31	LAN_RTL8111EPV	
32	RJ45&Transformer	
33	Card reader_(R)	
34	USB Charger_TPS2544	
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36	USB20_REAR PORT	
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38	USB30_REAR PORT	
39	USB30_(R)	
40	Power Plane EN Sequence	
41	Dual Power	
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43	DCIN JACK(BATT Conn)	
44	OZ554A LED Converter	
45	RT8243_5V/3D3V	
46	VCORE & V_GT IC (NCP81203)	
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49	DC to DC_12V (SY8246)	
50	MEM/MEMVTT (RT8207P)	
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53	VCC_IO(RT8237C)	
54	LDO_1P5V_1P8V_2P5V	

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63	SSD-NGFF	
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71	Thunderbolt_(R)	
72	Thunderbolt_(R)	
73	Thunderbolt_(R)	
74	Thunderbolt_(R)	
75	Thunderbolt_(R)	
76	GPU_(R)	
77	GPU_(R)	
78	GPU_(R)	
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87	GPU Switch_(R)	
88	GPU Switch_(R)	
89	GPU others_(R)	
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91	TPM	
92	PS2_(R)	
93	Express Card:PCIE X16	
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99	XDP&ITP	
100	Table of Content	
101	GPIO table	
102	POWER SEQUENCE	
103	Power Block Diagram	
104	SMBUS table	
105	CLOCK MAP	
106	RESET Flow CHART	
107	Change History	

PCB BOARD SIZE
6 Layers
200mmX240mm

BOM Configuration
Unmount:(R_)
Q170:(Q_)
H110:(H_)
VGA:(D_)
XDP:(X_)
3D WEBCAM:(W3_)
AMP:(A_)
SCALAR:(S_)
G-Sensor:(G_)
Non HDMI:(U_)
HDMI:(M)

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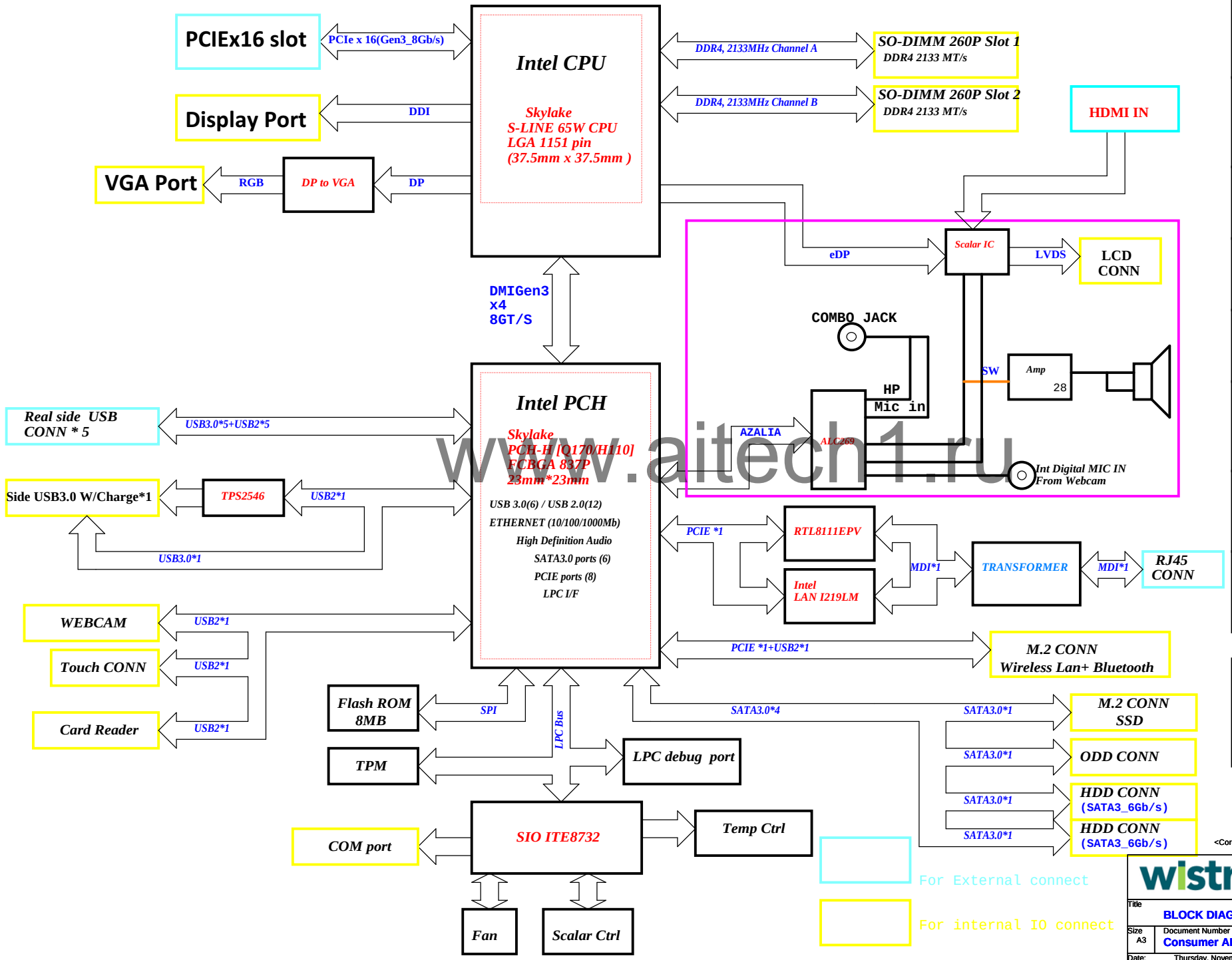
Title: COVER PAGE

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 1 of 107

Woody Block Diagram



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5V/3D3V DC/DC RT8243B	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_Charger 3D3V_A

CPU/GT DC/DC NCP81203	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE GFX_CORE

VCCSA DC/DC RT8237C	
INPUTS	OUTPUTS
DCBATOUT	VCC_SA

VCCIO DC/DC RT8237C	
INPUTS	OUTPUTS
DCBATOUT	VCC_IO

12V DC/DC RT8115C	
INPUTS	OUTPUTS
3D3V_S0	12V_S0

MEM/MEMVTT DC/DC RT8207P	
INPUTS	OUTPUTS
DCBATOUT	VDDQ 0D6V_VREF_S0

1D0V DC/DC RT8237C	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

VGA DC/DC NCP81172	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Bottom
L3:Signal	
L4:Signal	

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Title: BLOCK DIAGRAM

Size: A3 | Document Number: Consumer AIO Woody | Rev: SA

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2014/8/5
Change CPU P/N to 062.10015.0081

PEG

93 PEG_TX_CPU_P[0..15]
93 PEG_TX_CPU_N[0..15]
93 PEG_RX_CPU_P[0..15]
93 PEG_RX_CPU_N[0..15]

DMI

16 DMI_RX_CPU_P[0..3]
16 DMI_RX_CPU_N[0..3]
16 DMI_TX_CPU_P[0..3]
16 DMI_TX_CPU_N[0..3]

CPU1C 3 OF 12

SKYLAKE

LGA1151

PEG_RX_CPU_P0	B8	PEG_RXP0	PEG_TXP0	A5	PEG_TX_CPU_P0
PEG_RX_CPU_N0	B7	PEG_RXN0	PEG_TXN0	A6	PEG_TX_CPU_N0
PEG_RX_CPU_P1	C7	PEG_RXP1	PEG_TXP1	B4	PEG_TX_CPU_P1
PEG_RX_CPU_N1	C6	PEG_RXN1	PEG_TXN1	B5	PEG_TX_CPU_N1
PEG_RX_CPU_P2	D6	PEG_RXP2	PEG_TXP2	C3	PEG_TX_CPU_P2
PEG_RX_CPU_N2	D5	PEG_RXN2	PEG_TXN2	C4	PEG_TX_CPU_N2
PEG_RX_CPU_P3	E5	PEG_RXP3	PEG_TXP3	D2	PEG_TX_CPU_P3
PEG_RX_CPU_N3	E4	PEG_RXN3	PEG_TXN3	D3	PEG_TX_CPU_N3
PEG_RX_CPU_P4	F6	PEG_RXP4	PEG_TXP4	E1	PEG_TX_CPU_P4
PEG_RX_CPU_N4	F5	PEG_RXN4	PEG_TXN4	E2	PEG_TX_CPU_N4
PEG_RX_CPU_P5	G5	PEG_RXP5	PEG_TXP5	F2	PEG_TX_CPU_P5
PEG_RX_CPU_N5	G4	PEG_RXN5	PEG_TXN5	F3	PEG_TX_CPU_N5
PEG_RX_CPU_P6	H6	PEG_RXP6	PEG_TXP6	G1	PEG_TX_CPU_P6
PEG_RX_CPU_N6	H5	PEG_RXN6	PEG_TXN6	G2	PEG_TX_CPU_N6
PEG_RX_CPU_P7	J5	PEG_RXP7	PEG_TXP7	H2	PEG_TX_CPU_P7
PEG_RX_CPU_N7	J4	PEG_RXN7	PEG_TXN7	H3	PEG_TX_CPU_N7
PEG_RX_CPU_P8	K6	PEG_RXP8	PEG_TXP8	J1	PEG_TX_CPU_P8
PEG_RX_CPU_N8	K5	PEG_RXN8	PEG_TXN8	J2	PEG_TX_CPU_N8
PEG_RX_CPU_P9	L5	PEG_RXP9	PEG_TXP9	K2	PEG_TX_CPU_P9
PEG_RX_CPU_N9	L4	PEG_RXN9	PEG_TXN9	K3	PEG_TX_CPU_N9
PEG_RX_CPU_P10	M6	PEG_RXP10	PEG_TXP10	L1	PEG_TX_CPU_P10
PEG_RX_CPU_N10	M5	PEG_RXN10	PEG_TXN10	L2	PEG_TX_CPU_N10
PEG_RX_CPU_P11	N5	PEG_RXP11	PEG_TXP11	M2	PEG_TX_CPU_P11
PEG_RX_CPU_N11	N4	PEG_RXN11	PEG_TXN11	M3	PEG_TX_CPU_N11
PEG_RX_CPU_P12	P6	PEG_RXP12	PEG_TXP12	N1	PEG_TX_CPU_P12
PEG_RX_CPU_N12	P5	PEG_RXN12	PEG_TXN12	N2	PEG_TX_CPU_N12
PEG_RX_CPU_P13	R5	PEG_RXP13	PEG_TXP13	P2	PEG_TX_CPU_P13
PEG_RX_CPU_N13	R4	PEG_RXN13	PEG_TXN13	P3	PEG_TX_CPU_N13
PEG_RX_CPU_P14	T6	PEG_RXP14	PEG_TXP14	R2	PEG_TX_CPU_P14
PEG_RX_CPU_N14	T5	PEG_RXN14	PEG_TXN14	R1	PEG_TX_CPU_N14
PEG_RX_CPU_P15	U5	PEG_RXP15	PEG_TXP15	T2	PEG_TX_CPU_P15
PEG_RX_CPU_N15	U4	PEG_RXN15	PEG_TXN15	T3	PEG_TX_CPU_N15

VCC_IO
R301
1 PEG_RCOMP_CPU L7
PEG_RCOMP
24D9R2F-L-GP

DMI_RX_CPU_P0	Y3	DMI_RXP0	DMI_TXP0	AC2	DMI_TX_CPU_P0
DMI_RX_CPU_N0	Y4	DMI_RXN0	DMI_TXN0	AC1	DMI_TX_CPU_N0
DMI_RX_CPU_P1	AA4	DMI_RXP1	DMI_TXP1	AD3	DMI_TX_CPU_P1
DMI_RX_CPU_N1	AA5	DMI_RXN1	DMI_TXN1	AD2	DMI_TX_CPU_N1
DMI_RX_CPU_P2	AB4	DMI_RXP2	DMI_TXP2	AE2	DMI_TX_CPU_P2
DMI_RX_CPU_N2	AB3	DMI_RXN2	DMI_TXN2	AE1	DMI_TX_CPU_N2
DMI_RX_CPU_P3	AC4	DMI_RXP3	DMI_TXP3	AF2	DMI_TX_CPU_P3
DMI_RX_CPU_N3	AC5	DMI_RXN3	DMI_TXN3	AF3	DMI_TX_CPU_N3

GP

SKYLAKE-1

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Title: CPU(PCIE/DMI)
Size: Custom
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015 Sheet 3 of 107

CPU XDP

4 XDP_PCUDEBUG3

20 H_TCK

65 H_TRST_N

SVID

46 VIDSCK_VR1

46 VIDSOUT_VR1

46 VIDALERT#_VR1

CLOCK

18 CPU_BCLK_PCH

18 CPU_BCLK_PCH#

18 CPU_PCIBCLK_PCH

18 CPU_PCIBCLK_PCH#

18 CPU_CLK24M_PCH

18 CPU_CLK24M_PCH#

CONTROL

65 CPU_VCCST_PWRGD_R

43,46 PROCHOT#_R

40,50 DDR_VTT_CNTL

40 CPU_VCCST_PWRGD

20,65 H_PWRGD

17,65 PLTRST_CPU_N

17 PM_SYNC_CPU

17 PM_DOWN_PCH

17,24 PECI_CPU

17 THERMTRIP#_CPU_R

16 H_SKTOCC_N

20 PCH_JTAG_TDO

20 PCH_JTAG_TDI

20 PCH_JTAG_TMS

21 H_TRST_N_R

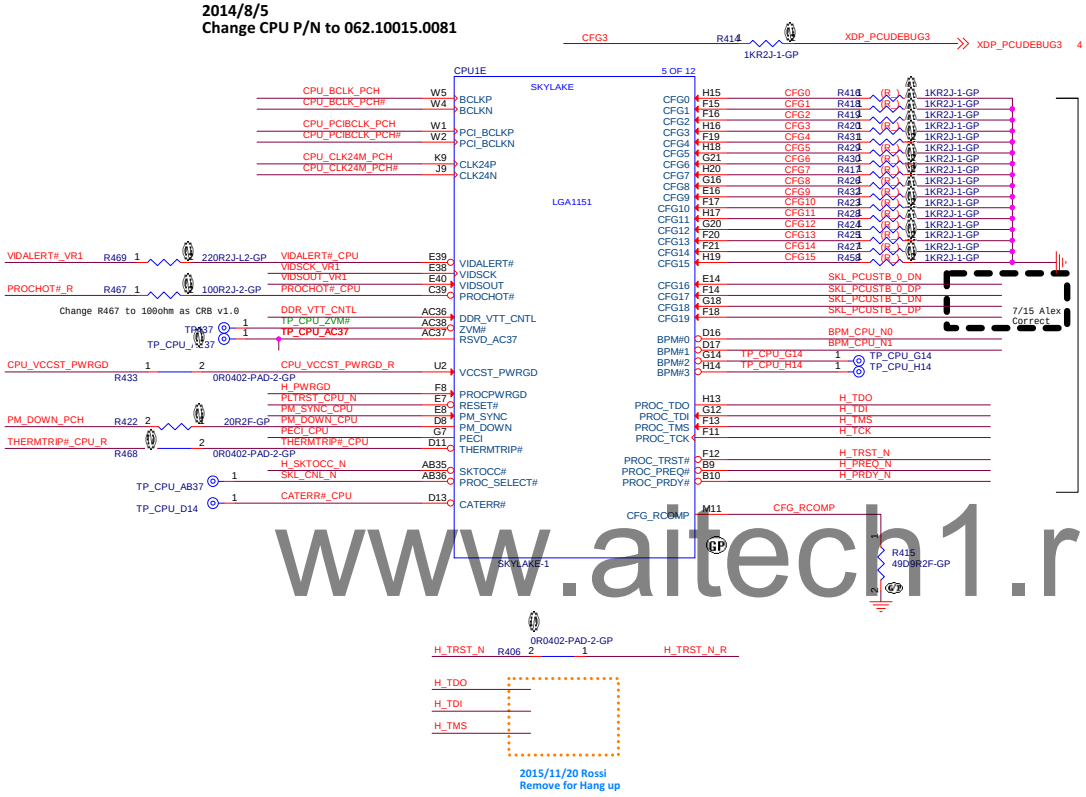
VIDSCK
VIDSOUT
VIDALERT#
Need to add Pull UP on both CPU and VR side.

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{ser1} [Ω]	R_{ser2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{GT} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

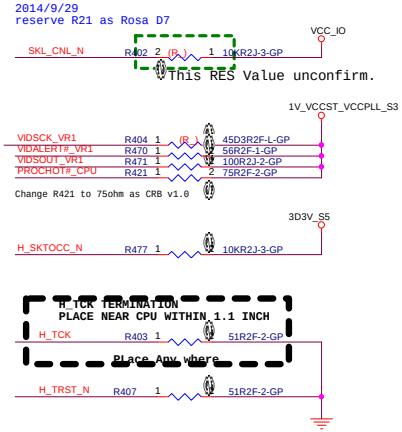
2014/9/29
reserve R21 as Rosa D7

This RES Value unconfirm.

2014/8/5
Change CPU P/N to 062.10015.0081



2015/11/20 Rossi
Remove for Hang up



- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

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Title: CPU_(THERMAL/CLOCK/PM/CFG)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

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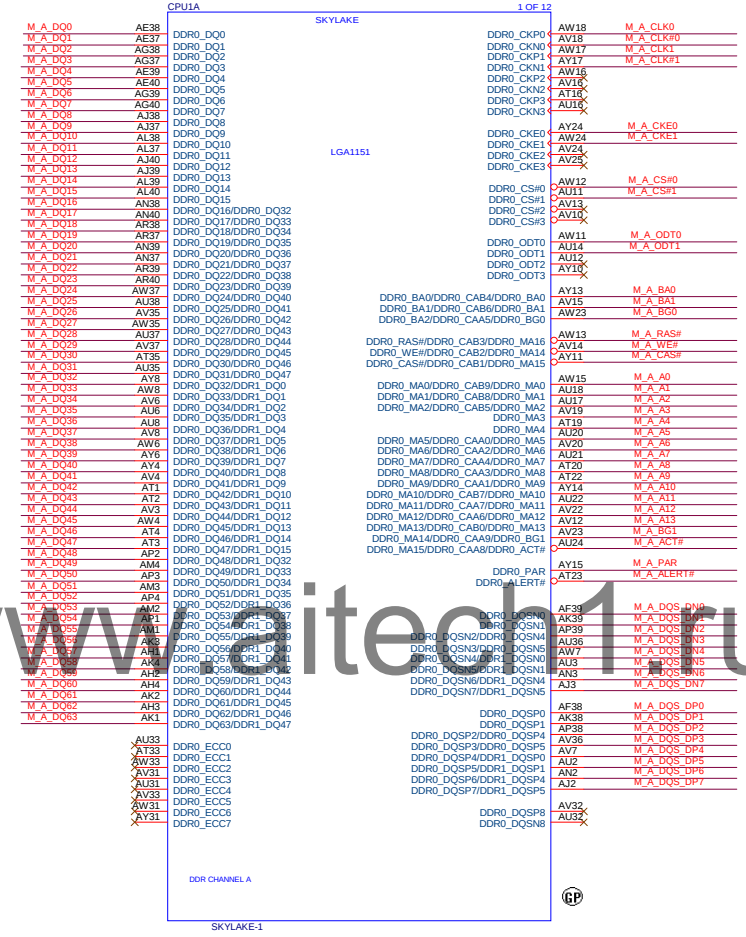
CHANNEL A DIMM0

11 M_A_DQ[63..0]
11 M_A_A[13..0]
11 M_A_DQS_DP[7..0]
11 M_A_DQS_DN[7..0]
11 M_A_BA[1..0]
11 M_A_BG[1..0]

11 M_A_CLK0
11 M_A_CLK#0
11 M_A_CLK1
11 M_A_CLK#1
11 M_A_CS#[1..0]

11 M_A_ACT#
11 M_A_ODT0
11 M_A_ODT1
11 M_A_CKE0
11 M_A_CKE1
11 M_A_CAS#
11 M_A_WE#
11 M_A_RAS#
11 M_A_ALERT#
11 M_A_PAR

2014/8/5
Change CPU P/N to 062.10015.0081



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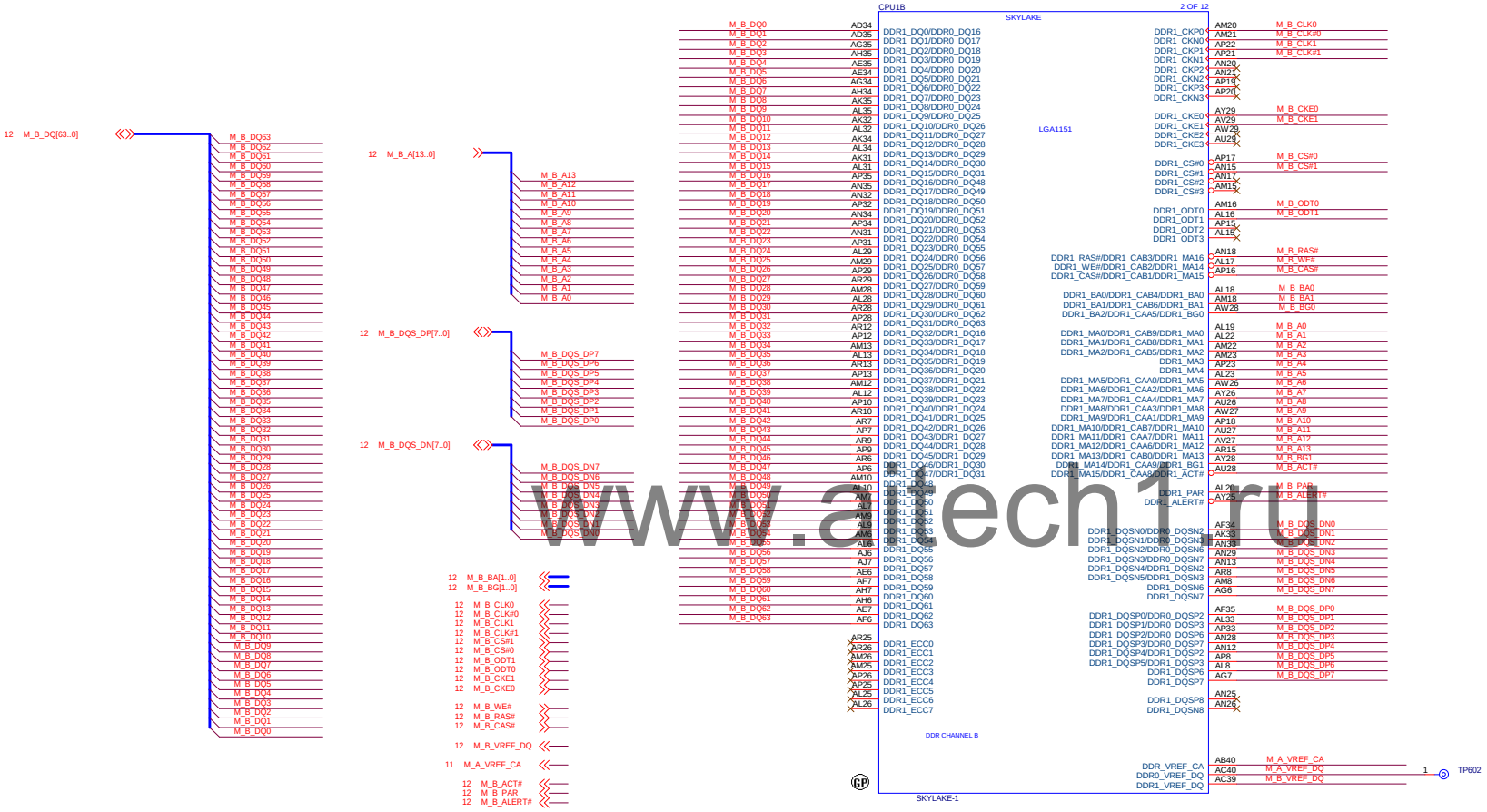
Title: CPU_(DDR4 CHANNEL A)
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA
Date: Thursday, November 26, 2015 | Sheet 5 of 107



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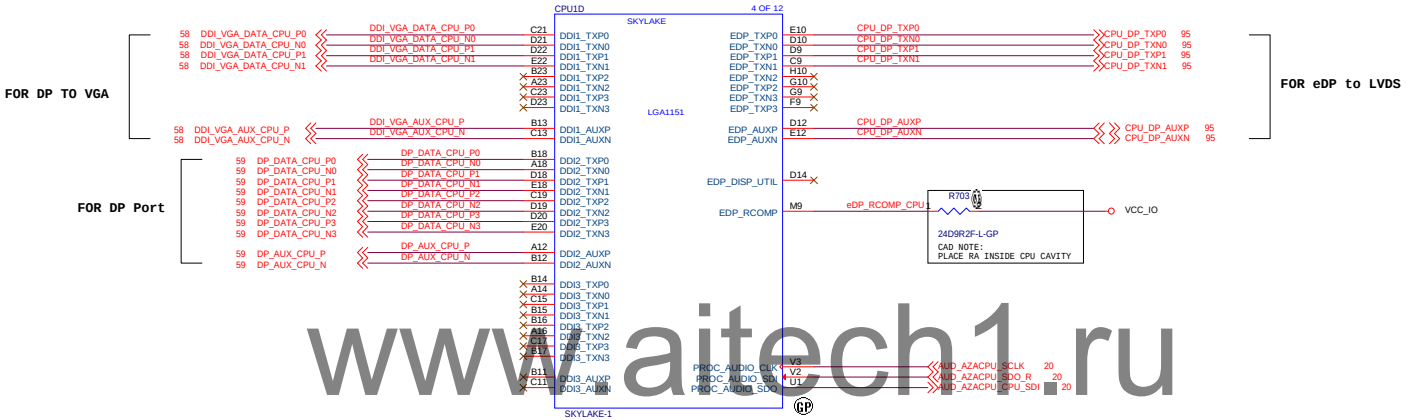
Title: CPU (DDR_CHB)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 6 of 107

2014/8/5
Change CPU P/N to 062.10015.0081



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Title	CPU (DDI/EDP)
Size: C	Document Number: Consumer AIO Woody
Rev: SA	
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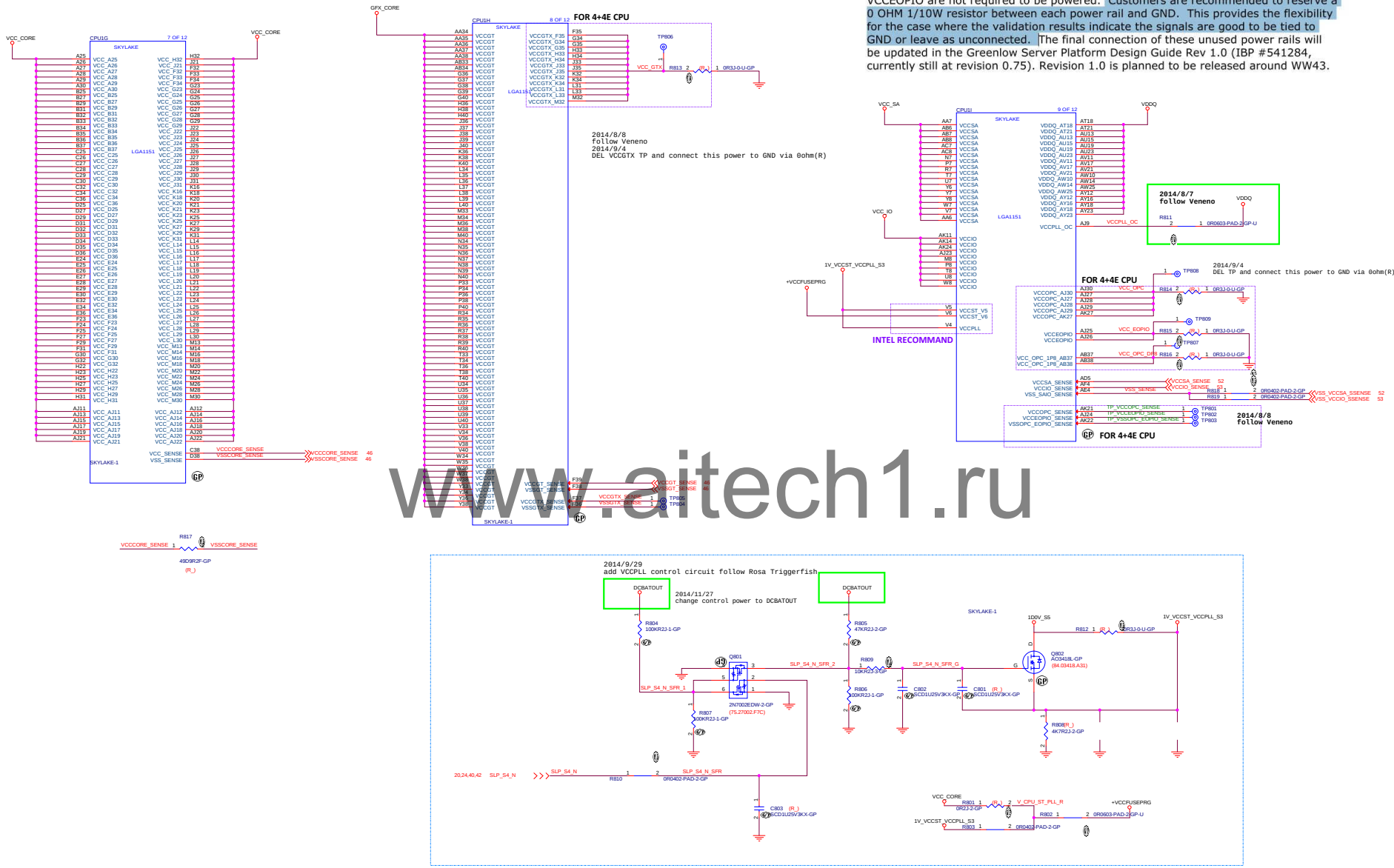
Greenlow Server Reference Circuit: Unused Power Pins Handling

Greenlow Server Reference board Zumba Beach does not support pGFX and EDRAM, hence some of the power rails such as VCCGT, VCCGTX, VCC_OPC_1P8, VCCOPC and VCCEOPIO are not required to be powered. Customers are recommended to reserve a 0 OHM 1/10W resistor between each power rail and GND. This provides the flexibility for the case where the validation results indicate the signals are good to be tied to GND or leave as unconnected. The final connection of these unused power rails will be updated in the Greenlow Server Platform Design Guide Rev 1.0 (IBP #541284, currently still at revision 0.75). Revision 1.0 is planned to be released around WW43.

2014/8/5
Change CPU P/N to 062.10015.0081



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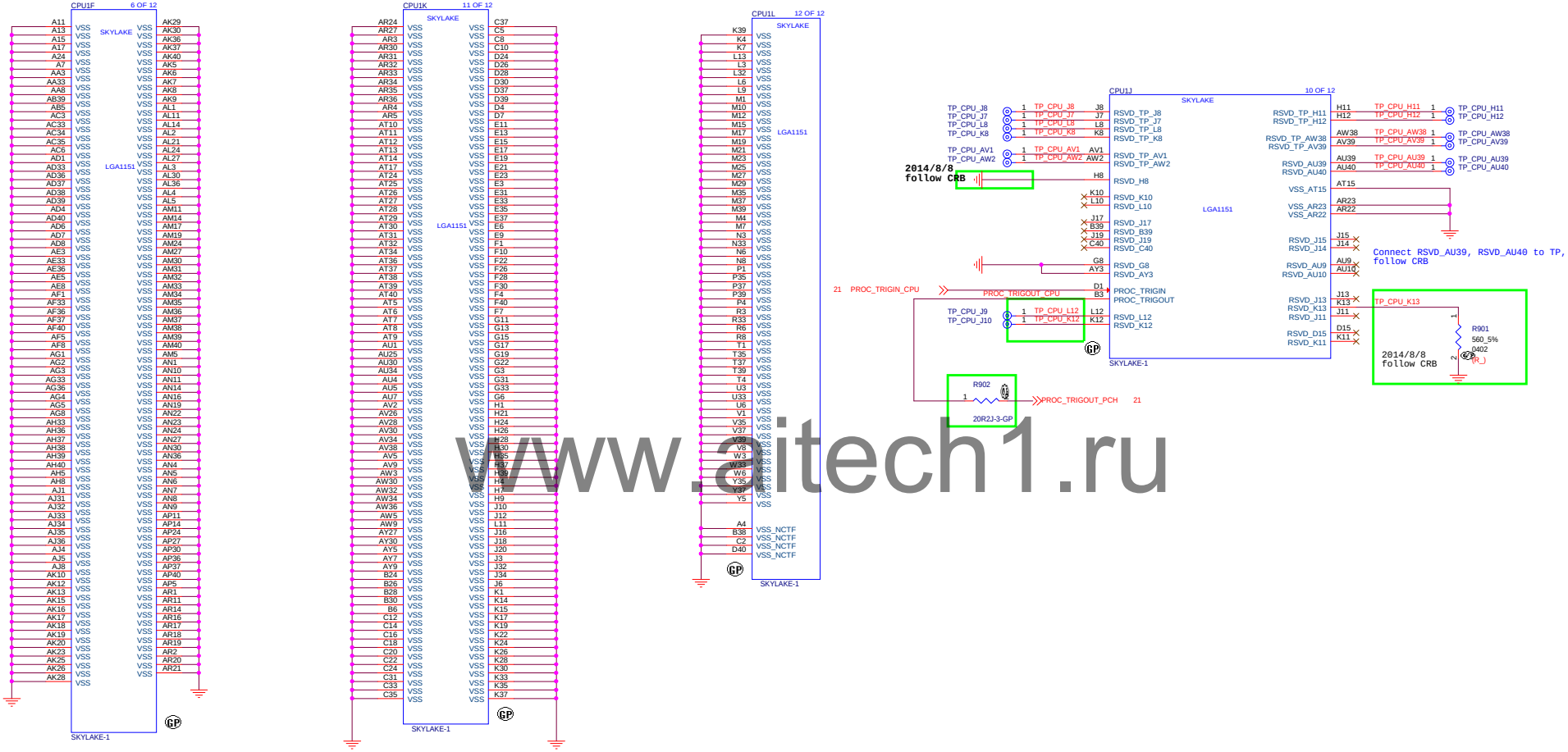
File: CPU (CPU Power)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 8 of 107

2014/8/5
Change CPU P/N to 062.10015.0081



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Title: CPU (VSS)

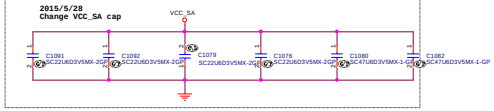
Size: C | Document Number: Consumer AIO Woody | Rev: SA

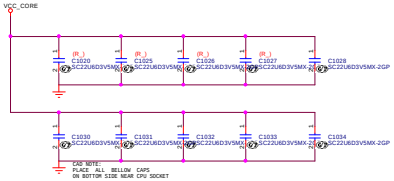
Date: Thursday, November 26, 2015 | Sheet 9 of 107

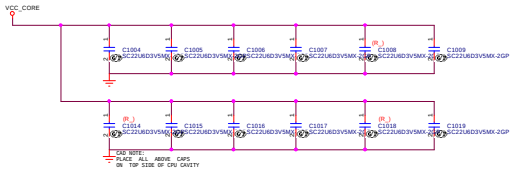
2014/8/8
DEL VCCOPC and VCCEOPIO power cap

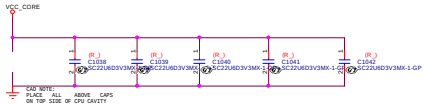
PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE

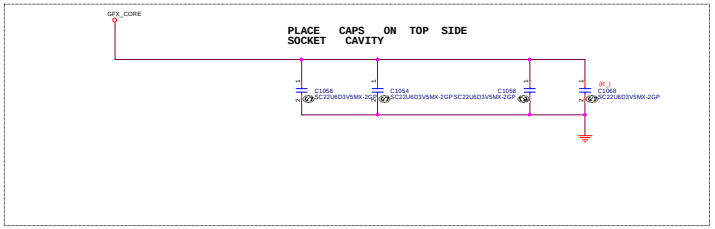
2015/5/28
Change VCC_SA cap

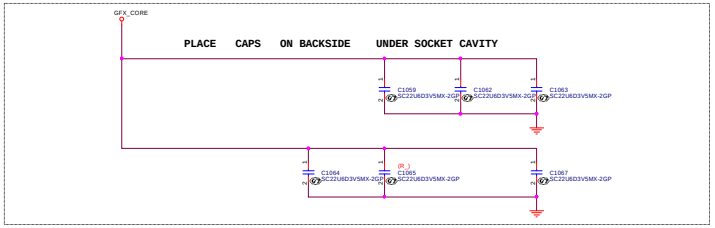


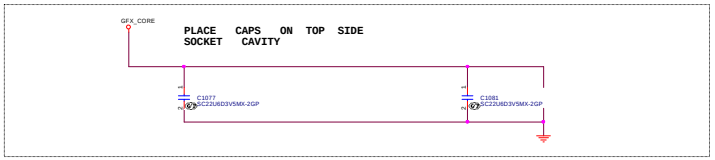






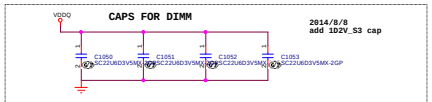




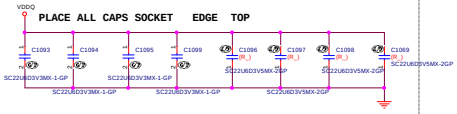


VDDQ
CAPS FOR DIMM

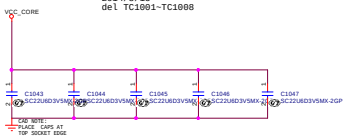
2014/8/8
add 1D2V_S3 cap



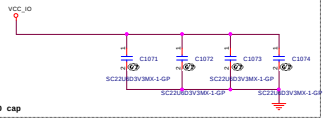
VDDQ
PLACE ALL CAPS SOCKET EDGE TOP



2014/8/15
del TC1001~TC1008

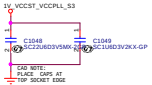


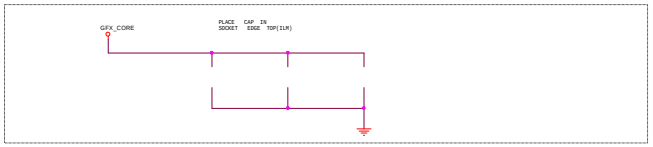
PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE

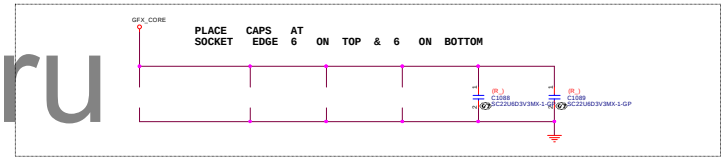


2014/8/8
add VCC_IO cap

PLACE ALL CAPS OUTSIDE CPU SOCKET CAVITY ON TOPSIDE







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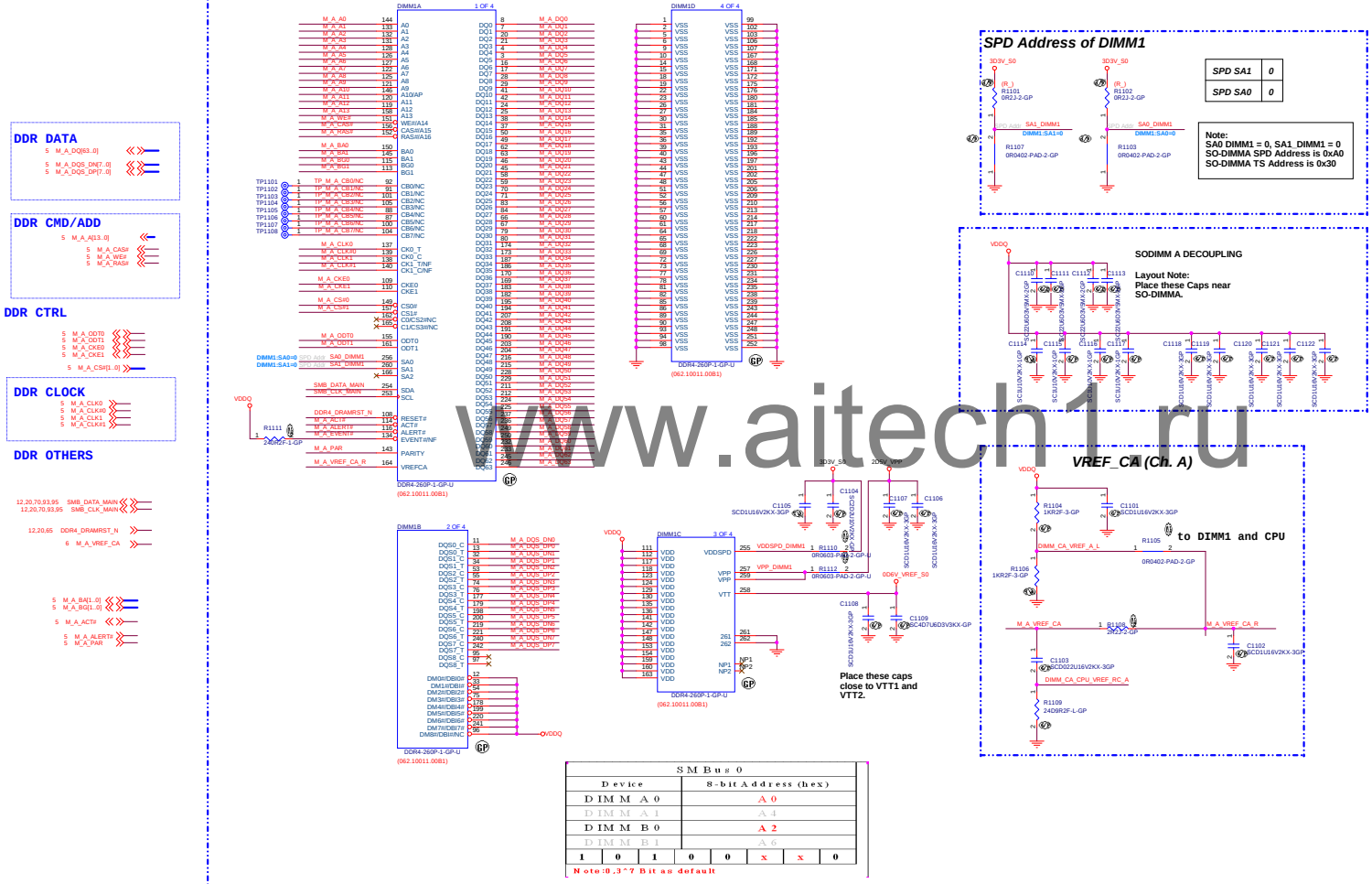
Hsichih, Taipei Hsien

Title: CPU Power CAP
Size: Custom
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 28, 2013
Sheet 10 of 107

CHANNEL-A XMM1, A0, H=9.2mm



SM Bus 0							
Device	8-bit Address (hex)						
DIMM A0	A0						
DIMM A1	A4						
DIMM B0	A2						
DIMM B1	A6						
1	0	1	0	0	x	x	0

Note:0,3^7 Bit as default

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Wistron Incorporated
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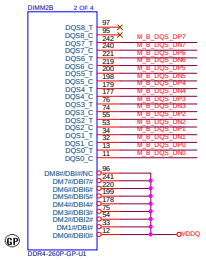
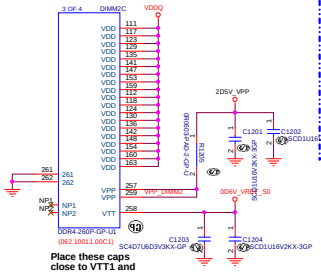
File: DDR4 DIMM_1
Size: Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015 Sheet 11 of 107

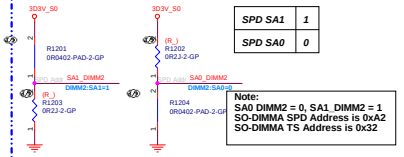
CHANNEL-B DIMM2, A2, H=5.2mm





Place these caps close to VTT1 and VTT2.

SPD Address of DIMM2

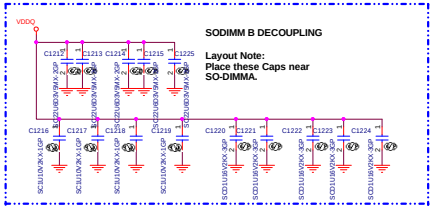


SPD SA1	1
SPD SA0	0

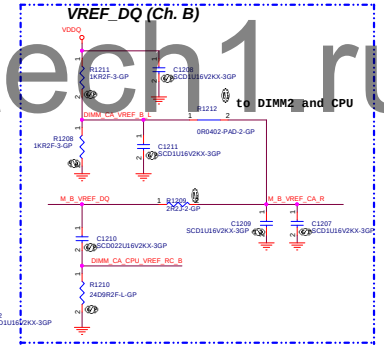
Note:
SA0 DIMM2 = 0, SA1_DIMM2 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.



VREF_DQ (Ch. B)



SM Bus 0							
Device	8-bit Address (hex)						
DIMM A0	A0						
DIMM A1	A4						
DIMM B0	A2						
DIMM B1	A6						
1	0	1	0	0	x	x	0

Note: 0,3~7 Bit as default

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File: DDR4 DIMM_2
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA
Date: Thursday, November 26, 2015 | Sheet 12 of 107

Reserved

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Title: DDR4 DIMM_3_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 13 of 107

Reserved

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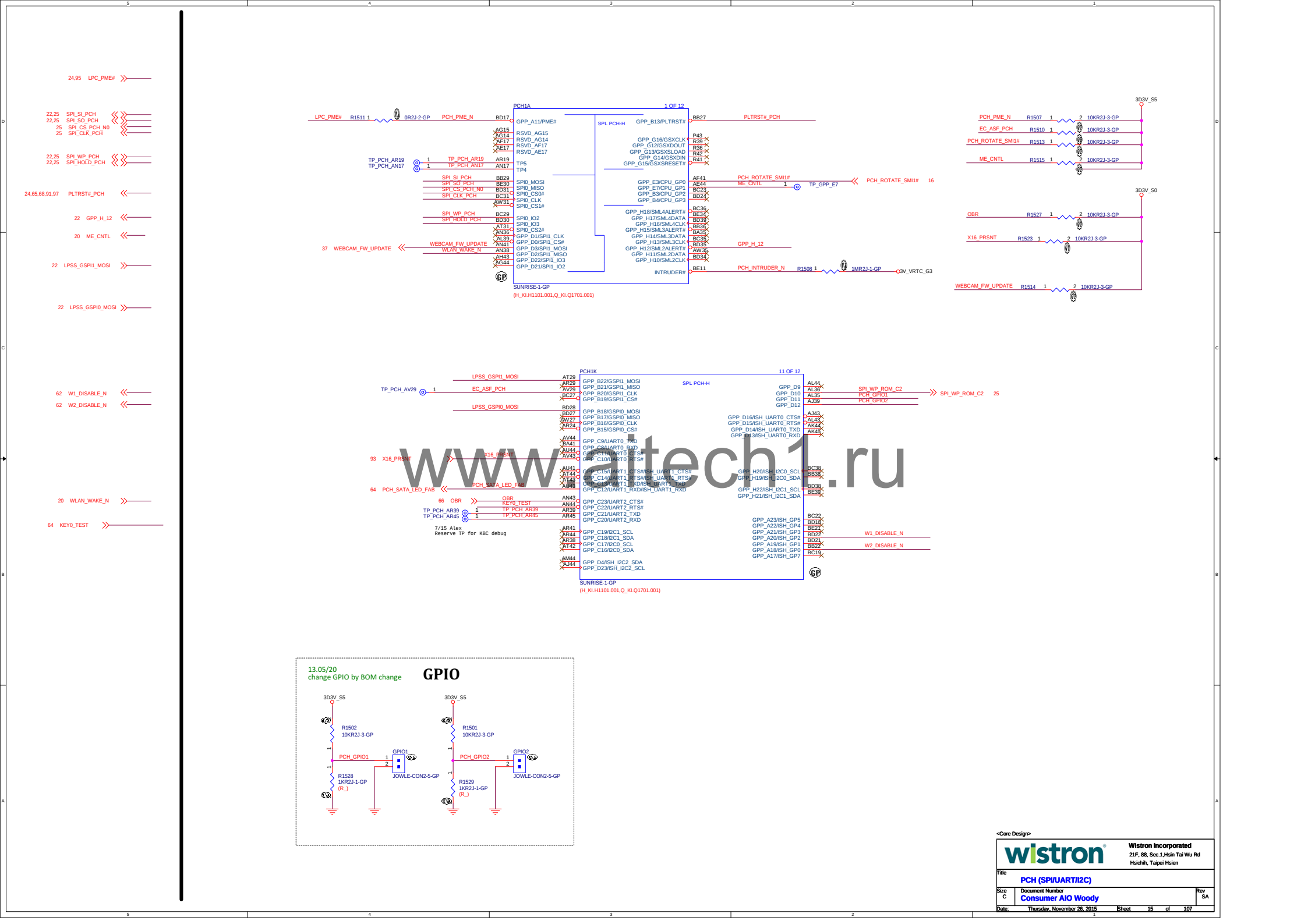
Title: DDR4 DIMM_4_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 14 of 107


24,95 LPC_PME#
22,25 SPI_SI_PCH
22,25 SPI_SO_PCH
25 SPI_CS_PCH_N0
25 SPI_CLK_PCH
22,25 SPI_WP_PCH
22,25 SPI_HOLD_PCH
24,65,68,91,97 PLTRST#_PCH
22 GPP_H_12
20 ME_CNTL
22 LPSS_GSPI1_MOSI
22 LPSS_GSPI0_MOSI
62 W1_DISABLE_N
62 W2_DISABLE_N
20 WLAN_WAKE_N
64 KEY0_TEST
PCH1A
1 OF 12
SUNRISE-1-GP
(H_KI.H1101.001.Q_KI.Q1701.001)
PCH1K
11 OF 12
SUNRISE-1-GP
(H_KI.H1101.001.Q_KI.Q1701.001)
3D3V_S5
3D3V_S0
13.05/20
change GPIO by BOM change
GPIO
JOWLE-CON2-5-GP
7/15 Alex
Reserve TP for KBC debug
<Core Design>
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
PCH (SPI/UART/I2C)
Consumer AIO Woody
Thursday, November 26, 2015
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DMI

3 DMI_TX_CPU_N[0..3]
3 DMI_TX_CPU_P[0..3]
3 DMI_RX_CPU_N[0..3]
3 DMI_RX_CPU_P[0..3]

USB Table

Pair	Device
1	USB3.0 Ext. port 1 (Side)
2	USB3.0 Ext. port 2 (Rear)
3	USB3.0 Ext. port 3 (Rear)
4	USB3.0 Ext. port 4 (Rear)
5	USB3.0 Ext. port 5 (Rear)
6	USB2.0 Ext. port 5 (Rear)
7	WLAN+BT
8	WEB CAM(Front)
9	CR Ext. Header (Side)
10	TOUCH
11	Internal USB connector
12	Internal USB connector
13	TBD
14	TBD

PCH1B — 2 OF 12 — SPL PCH-H — DMI — USB 2.0 — PCH1B3 — SUNRISE-1-GP

DMI_TX_CPU_N0 L27 / DMI_TX_CPU_P0 N27 / DMI_RX_CPU_N0 C27 / DMI_RX_CPU_P0 B27 / DMI_TX_CPU_N1 E24 / DMI_TX_CPU_P1 G24 / DMI_RX_CPU_N1 B28 / DMI_RX_CPU_P1 A28 / DMI_TX_CPU_N2 G27 / DMI_TX_CPU_P2 E26 / DMI_RX_CPU_N2 B29 / DMI_RX_CPU_P2 C29 / DMI_TX_CPU_N3 L29 / DMI_TX_CPU_P3 K29 / DMI_RX_CPU_N3 B30 / DMI_RX_CPU_P3 A30
DMI_RXN0 DMI_RXP0 DMI_TXN0 DMI_TXP0 DMI_RXN1 DMI_RXP1 DMI_TXN1 DMI_TXP1 DMI_RXN2 DMI_RXP2 DMI_TXN2 DMI_TXP2 DMI_RXN3 DMI_RXP3 DMI_TXN3 DMI_TXP3

0402 100 1% 1 R1608 — PEG_RCOMPN_CPU B18 / PEG_RCOMPP_CPU C17 — PCIE_RCOMPN PCIE_RCOMPP

PCIE1_RXN/USB3_7_RXN H15 / PCIE1_RXP/USB3_7_RXP G15 / PCIE1_TXN/USB3_7_TXN A16 / PCIE1_TXP/USB3_7_TXP B16
PCIE2_TXN/USB3_8_TXN B19 / PCIE2_TXP/USB3_8_TXP C19 / PCIE2_RXN/USB3_8_RXN E17 / PCIE2_RXP/USB3_8_RXP G17
PCIE3_RXN/USB3_9_RXN L17 / PCIE3_RXP/USB3_9_RXP K17 / PCIE3_TXN/USB3_9_TXN B20 / PCIE3_TXP/USB3_9_TXP C20
PCIE4_RXN/USB3_10_RXP E20 / PCIE4_RXP/USB3_10_RXN G19 / PCIE4_TXN/USB3_10_TXN B21 / PCIE4_TXP/USB3_10_TXP A21
PCIE5_RXN K19 / PCIE5_RXP L19 / PCIE5_TXN D22 / PCIE5_TXP C22
PCIE6_RXN G22 / PCIE6_RXP F22 / PCIE6_TXN B22 / PCIE6_TXP A23
PCIE7_RXN C23 / PCIE7_RXP K22 / PCIE7_TXN L22 / PCIE7_TXP B23
PCIE8_RXN K24 / PCIE8_RXP L24 / PCIE8_TXN B24 / PCIE8_TXP C24

(H_KI.H1101.001.Q_KI.Q1701.001)

USB2N_1 AF5 / USB2P_1 AG7 / USB2N_2 AD5 / USB2P_2 AD7 / USB2N_3 AG8 / USB2P_3 AG10 / USB2N_4 AE1 / USB2P_4 AE2 / USB2N_5 AC2 / USB2P_5 AC3 / USB2N_6 AF2 / USB2P_6 AF3 / USB2N_7 AB3 / USB2P_7 AB2 / USB2N_8 AL8 / USB2P_8 AL7 / USB2N_9 AA1 / USB2P_9 AA2 / USB2N_10 AJ8 / USB2P_10 AJ7 / USB2N_11 W2 / USB2P_11 W3 / USB2N_12 AD3 / USB2P_12 AD2 / USB2N_13 V2 / USB2P_13 V1 / USB2N_14 AJ11 / USB2P_14 AJ13

USB_PCH_PN1 … USB_PCH_PN12 / USB_PCH_PP1 … USB_PCH_PP12

GPP_E9/USB2_OC0# AD43 / GPP_E10/USB2_OC1# AD42 / GPP_E11/USB2_OC2# AD39 / GPP_E12/USB2_OC3# AC44 / GPP_F15/USB2_OCB_4 Y43 / GPP_F16/USB2_OCB_5 Y41 / GPP_F17/USB2_OCB_6 W44 / GPP_F18/USB2_OCB_7 W43

CHARGER_OC_2# 34 / USB30_OC_P1# 42 / USB30_OC_P2# 42 / VSACH2_D3 22 / USB30_OC_P4# 42
USB2_OCB_5 / USB2_OCB_6 / USB2_OCB_7

USB2_COMP AG3 / USB2_VBUSSENSE AD10 / RSVD_AB13 AB13 / USB2_ID AG2
R1604 1 — 113R2F-GP — USB2_COMP
R1605 1 — 1KR2J-1-GP — USB2_VBUSSENSE
TP_PCH_AB13
R1606 1 — 1KR2J-1-GP — USB2_ID

GPD7/RSVD BD14 — EDID_RDY — EDID_RDY 17,95

LAN

31,97 PCIE_TX_LAN_N5 / 31,97 PCIE_TX_LAN_P5 — PCIE_TX_LAN_N5 / PCIE_TX_LAN_P5 — C1614 / C1613 — SCD1U16V2KX-3GP — PCIE_RX_LAN_N5 / PCIE_RX_LAN_P5 — PCIE_TX_PCH_N5 / PCIE_TX_PCH_P5

WLAN

62 PCIE_TX_WLAN_N7 / 62 PCIE_TX_WLAN_P7 — PCIE_TX_WLAN_N7 / PCIE_TX_WLAN_P7 — C1615 / C1616 — SCD1U16V2KX-3GP — 62 PCIE_RX_PCH_N7 / 62 PCIE_RX_PCH_P7 — PCIE_RX_PCH_N7 / PCIE_RX_PCH_P7 — PCIE_TX_PCH_N7 / PCIE_TX_PCH_P7

3D Webcam ASM1042A

37 PCIE_TX_CAM_N8 / 37 PCIE_TX_CAM_P8 — PCIE_TX_CAM_N8 / PCIE_TX_CAM_P8 — C1618 / C1617 — SCD1U16V2KX-3GP — 37 PCIE_RX_PCH_N8 / 37 PCIE_RX_PCH_P8 — PCIE_RX_PCH_N8 / PCIE_RX_PCH_P8 — PCIE_TX_PCH_N8 / PCIE_TX_PCH_P8

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BOARD ID

3D3V_S5

R1601 10KR2J-3-GP (R_) — BOARD_ID_2
R1616 10KR2J-3-GP (U_) — BOARD_ID_1
R1618 10KR2J-3-GP (Q_) — BOARD_ID_0
R1619 10KR2J-3-GP — R1615 10KR2J-3-GP (M_) — R1617 10KR2J-3-GP (H_)

SB EC Board ID Description

H110	ID2 bit1	ID1 bit0
W/HDMI	0	0
W/O HDMI	0	1

	ID0
Q170	1
H110	0

CHARGER_OC_2# / USB2_OCB_5 — RN1609 — SRN2K2J-1-GP
USB2_OCB_6 / USB2_OCB_7 — RN1608 — SRN2K2J-1-GP
3D_WEBCAM_PWR_CRL1 — R1625 10KR2J-3-GP
PCH_EC_SMI1# — R1621 10KR2J-3-GP — 3D3V_S0
DPB_CTRLCLK_PCH / DPB_CTRLDATA_PCH — RN1610 — SRN2K2J-1-GP

PCH1E — 5 OF 12 — SPL PCH-H — SUNRISE-1-GP

R1627 0R0402-PAD-2-GP — 58 CRT_HPD_PCH / 59 DP_HPD_PCH — DDPE_HPD / DP_HPD_PCH / PCH_EC_SMI1# — AW4 / AY2 / AV4 / BA4
R1626 100KR2J-1-GP (R_)
R1620 0R0402-PAD-2-GP — 95 DP_HPD_N — EDP_HPD — BD7

GPP_I0/DDPB_HPD0 / GPP_I1/DDPC_HPD1 / GPP_I2/DDPD_HPD2 / GPP_I3/DDPE_HPD3 / GPP_I4/EDP_HPD

GPP_I7/DDPC_CTRLCLK BB3 / GPP_I8/DDPC_CTRLDATA BD6 / GPP_I5/DDPB_CTRLCLK BA5 / GPP_I6/DDPB_CTRLDATA BC4 / GPP_I9/DDPD_CTRLCLK BE5 / GPP_I10/DDPD_CTRLDATA BE6
DPC_CTRLCLK_PCH / DPC_CTRLDATA_PCH / DPB_CTRLCLK_PCH / DPB_CTRLDATA_PCH
DPC_CTRLCLK_PCH 59 / DPC_CTRLDATA_PCH 59

GPP_F14 Y44 / GPP_F23 V44 / GPP_F22 W38 — H_SKTOCC_N 4
GPP_G23 L43 / GPP_G22 L44 / GPP_G21 U35 / GPP_G20 R35 / GPP_H23 BD36 — BOARD_ID_2 / BOARD_ID_1 / BOARD_ID_0 / 3D_WEBCAM_PWR_CRL1 — 3D_WEBCAM_PWR_CRL1 37

(H_KI.H1101.001.Q_KI.Q1701.001)

3D3V_S0 — R1624 10KR2J-3-GP — EC_SMI1_EN
24 EC_SMI# — EC_SMI# — PCH_ROTATE_SMI1# — PCH_ROTATE_SMI1# 15
Q1601 2N7002KDW-GP (75.27002.F7C)
PCH_EC_SMI1# — EC_ROTATE_SMI1# — EC_ROTATE_SMI1# 24
EC_SMI1_EN

<Core Design>

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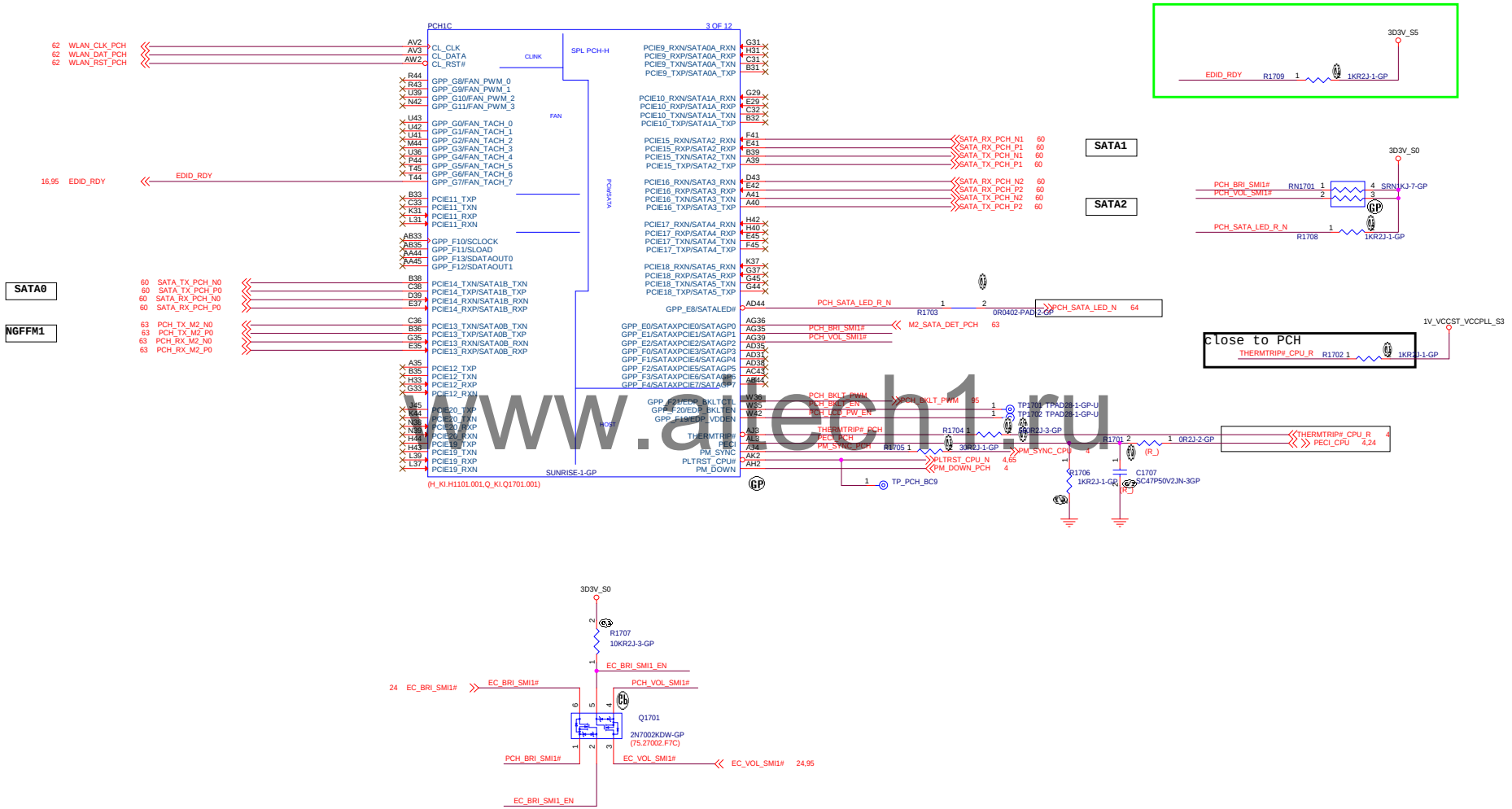
Hsichih, Taipei Hsien

Title: PCH (DMI/PCI-E/USB)
Size: C — Document Number: Consumer AIO Woody — Rev: SA
Date: Thursday, November 26, 2015 — Sheet 16 of 107



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Hsichih, Taipei Hsien

Title: PCH (PCI-E/SATA)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 17 of 107

6/21 Delete
CLKOUT_48 is only supported and enabled on SKL-H Server

2014/8/13 2.7K 1%
1V_VCCF24_Sx NEED CHECK
R1803 1 2K7R2F-GP
6/26 2.7K 0.5%
INTEL PDG: 2.71K 0.5%

TP_PCH_AR17 1 CLKOUT_48M_R

PCH1G 7 OF 12
AR17 GPP_A16/CLKOUT_48 SPL PCH-H

4 CPU_CLK24M_PCH G1 CLKOUT_CPUNSSC_P
4 CPU_CLK24M_PCH# F1 CLKOUT_CPUNSSC#
4 CPU_BCLK_PCH G2 CLKOUT_CPUBCLK_P
4 CPU_BCLK_PCH# H2 CLKOUT_CPUBCLK#
XTL_24M_OUT_PCH A5 XTAL24_OUT
XTL_24M_IN_PCH A6 XTAL24_IN
XCLK_BIASREF_PCH E1 XCLK_BIASREF
XTL_32K_X1_PCH BC9 RTCX1
XTL_32K_X2_PCH BD10 RTCX2

62 PEG_CLKREQ1_WLAN# BC24 GPP_B5/SRCCLKREQ0#
31,97 PEG_CLKREQ2_LAN# AW24 GPP_B6/SRCCLKREQ1#
AT24 GPP_B7/SRCCLKREQ2#
37 PEG_CLKREQ4_3D# BD25 GPP_B8/SRCCLKREQ3#
BB23 GPP_B9/SRCCLKREQ4#
BE25 GPP_B10/SRCCLKREQ5#
AT33 GPP_H0/SRCCLKREQ6#
63 PEG_CLKREQ7_M2# AR31 GPP_H1/SRCCLKREQ7#
93 PEG_CLKREQ8_PCIE16# BD33 GPP_H2/SRCCLKREQ8#
BC32 GPP_H3/SRCCLKREQ9#
BB31 GPP_H4/SRCCLKREQ10#
BC33 GPP_H5/SRCCLKREQ11#
BA33 GPP_H6/SRCCLKREQ12#
AW33 GPP_H7/SRCCLKREQ13#
BB33 GPP_H8/SRCCLKREQ14#
BD33 GPP_H9/SRCCLKREQ15#

PEG_CLKREQ7_M2#
PEG_CLKREQ8_PCIE16#

R13 R11 CLKOUT_PCIE_N15 CLKOUT_PCIE_P15
P1 R2 CLKOUT_PCIE_N14 CLKOUT_PCIE_P14
W1 Y3 CLKOUT_PCIE_N13 CLKOUT_PCIE_P13
U2 U3 CLKOUT_PCIE_N12 CLKOUT_PCIE_P12

SUNRISE-1-GP
(H_KI.H1101.001.Q_KI.Q1701.001)

CLKOUT_ITPXDP# L1 XDP_CLK_CON#
CLKOUT_ITPXDP_P L2 XDP_CLK_CON
CLKOUT_CPUPCIBCLK# J1 CPU_PCIBCLK_PCH# 4
CLKOUT_CPUPCIBCLK_P J2 CPU_PCIBCLK_PCH 4

CLKOUT_PCIE_N0 N7
CLKOUT_PCIE_P0 N8
CLKOUT_PCIE_N1 L7 PEG_CLK1_WLAN# 62
CLKOUT_PCIE_P1 L5 PEG_CLK1_WLAN 62
CLKOUT_PCIE_N2 D3 PEG_CLK2_LAN# 31,97
CLKOUT_PCIE_P2 F2 PEG_CLK2_LAN 31,97
CLKOUT_PCIE_N3 E5
CLKOUT_PCIE_P3 G4
CLKOUT_PCIE_N4 D5 PEG_CLK4_3D# 37
CLKOUT_PCIE_P4 E6 PEG_CLK4_3D 37
CLKOUT_PCIE_N5 D8
CLKOUT_PCIE_P5 D7
CLKOUT_PCIE_N6 R8
CLKOUT_PCIE_P6 R7
CLKOUT_PCIE_N7 U5 PEG_CLK7_M2# 63
CLKOUT_PCIE_P7 U7 PEG_CLK7_M2 63
CLKOUT_PCIE_N8 W10 PEG_CLK8_PCH# 93
CLKOUT_PCIE_P8 W11 PEG_CLK8_PCH 93
CLKOUT_PCIE_N9 N3
CLKOUT_PCIE_P9 N2
CLKOUT_PCIE_N10 P3
CLKOUT_PCIE_P10 P2
CLKOUT_PCIE_N11 T3
CLKOUT_PCIE_P11 R4

CLK OUT for CPU XDP
CLK OUT OF WLAN
CLK OUT OF PCIE for LAN
CLK OUT OF PCIE for 3D WEBCAM
CLK OUT OF NGFF for SSD
CLK OUT OF PCIE for PCIEX16

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XTL_32K_X1_PCH
R1808 1 10MR3J-L1-GP XTL_32K_X2_PCH
X1801 XTAL-32D768KHZ-64-GP
C1801 SC4P50V2CN-GP (78.4R074.1FL)
C1804 SC4P50V2CN-GP (78.4R074.1FL)
82.30001.661

XTL_24M_IN_PCH
R1807 1MR2J-1-GP
X1802 XTAL-24MHZ-126-GP
C1802 SC8P50V2CN-3GP (78.27034.1FL)
C1803 SC8P50V2CN-3GP (78.27034.1FL)
XTL_24M_OUT_PCH

3D3V_S0
PEG_CLKREQ1_WLAN# R1809 10KR2J-3-GP
3D3V_S5
PEG_CLKREQ2_LAN# R1810 10KR2J-3-GP
3D3V_S0
PEG_CLKREQ7_M2# R1811 10KR2J-3-GP

<Core Design>

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21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH(CLOCK/CL)
Size: C
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PORT1 USB30 SIDE PORT

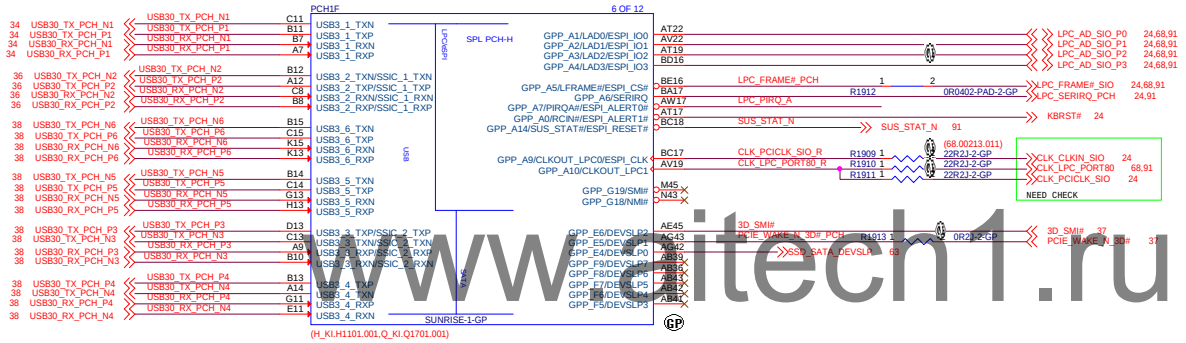
PORT2 USB30 REAR PORT

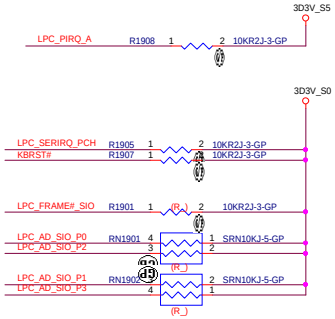
PORT6 USB30 REAR PORT

PORT5 USB30 REAR PORT

PORT3 USB30 REAR PORT

PORT4 USB30 REAR PORT





Integrated Pull-ups and Pull-downs

Signal	Resistor Type	Value	Notes
LAD[3:0]	Pull-up	15 - 40 KΩ	

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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (USB/ESPI

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 19 of 107

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Close to PCH

2014/9/29
R702 to 20ohm, follow CRB v1.0

2014/7/31
add SMLINK0 bus off page for Intel LAN

2015/11/18 Rossi
Change to bead for Hang up issue

CAD NOTE: PLACE CLOSE TO PCH

ME ENABLE /DISABLE

Flash Descriptor Security Overide
Low = Default High = Debug mode

need resume GPIO

CMOS CLR JUMPER

CRB pull 30.1k , but PDG use 20k

2014/8/1
change CMOS1 to 21.61445.103

2014/8/13
follow PDG

1-2 Normal
2-3 CLR CMOS

2014/8/9 add SMBus level shift
2014/10/14 modify SMBus as Madrid

84.2N702.A3F
2nd = 84.DM601.03F

check logic & current leakage

2014/8/22
reserve PD follow Lijiang

2014/10/10
add SUSCLK buffer

Follow GB

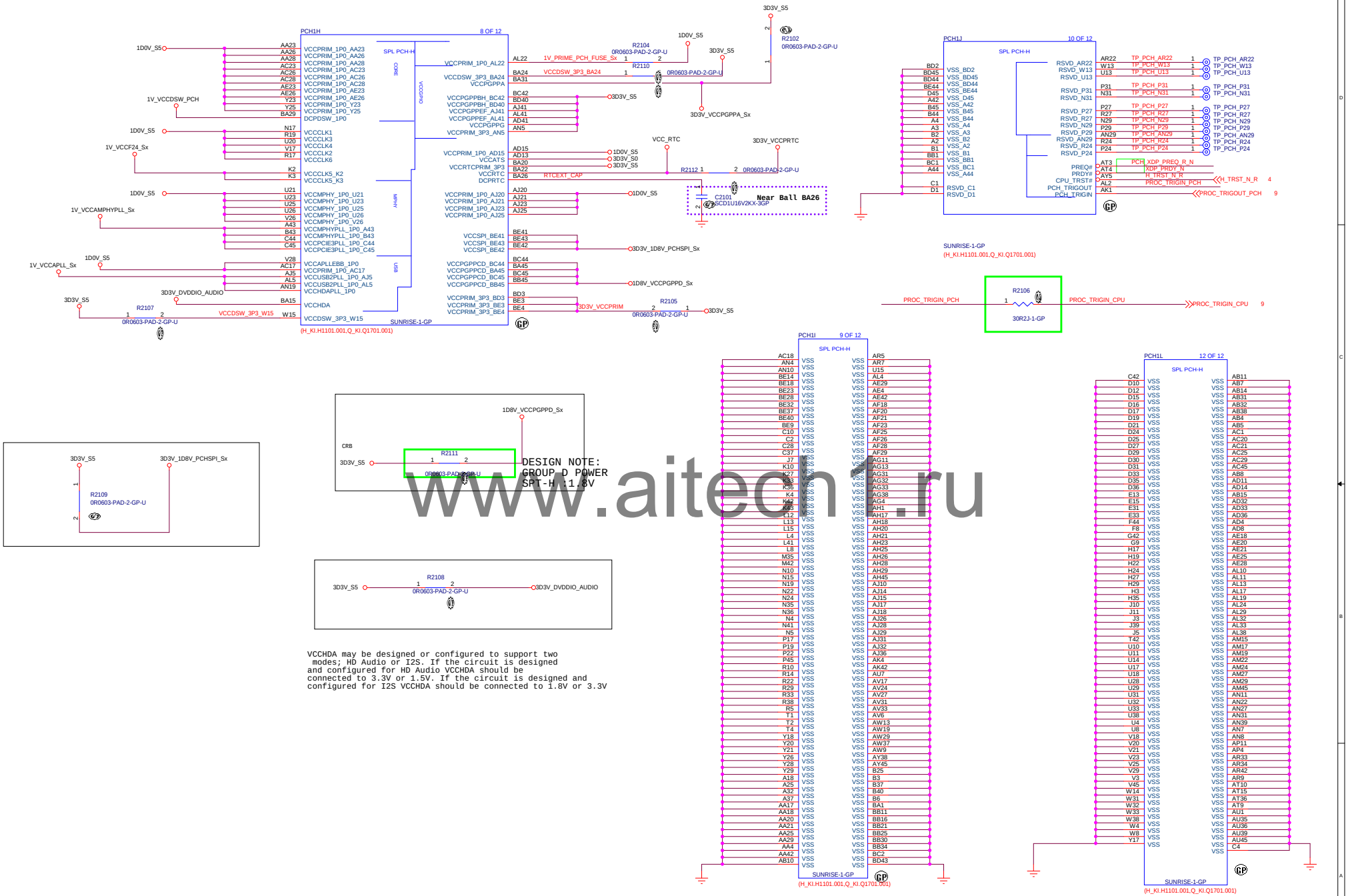
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (GPIO/CPU/SMBUS/IHDA/JTAG)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 20 of 107



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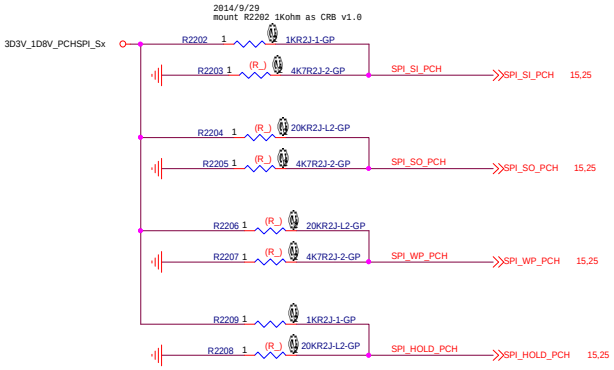
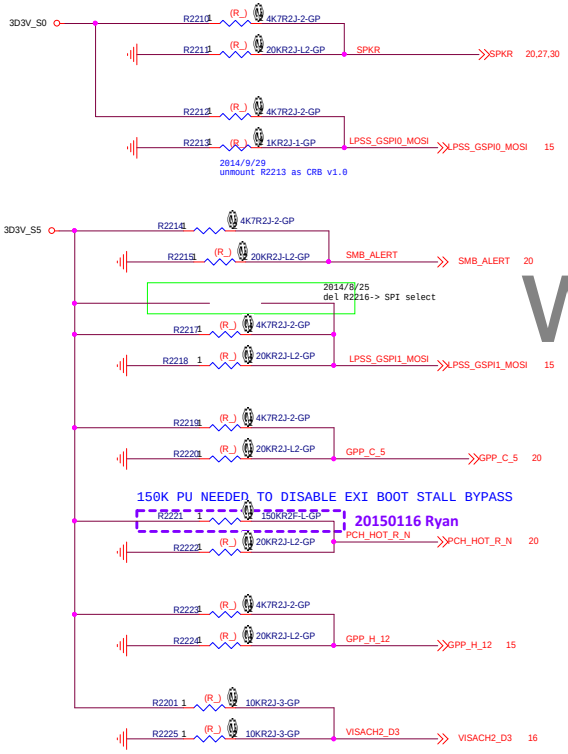
<Core Design>
wistron
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title: PCH (POWER1)
Size: C
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 21 of 107

PCH STRAP FUNCTIONS



SPI_SI_PCH (SPI0_MOSI)	0: Enable boot halt 1: Disable boot halt The internal PU resistor is enabled when RSMRST# is asserted and is switched to the internal PD when RSMRST# is de-asserted.
SPI_SO_PCH (SPI0_MISO)	0: Disable JTAG ODT 1: Enable JTAG ODT The internal PU resistor is enabled when RSMRST# is asserted
SPI_WP_PCH (SPI0_IO2)	0: Enable consent strap 1: Disable consent strap PCH has internal weak PU
SPI_HOLD_PCH (SPI0_IO3)	0: Enable personality strap 1: Disable personality strap PCH has internal weak PU



SPKR (SPKR / GPP_B14)	0: Disable Top Swap mode. (Default) 1: Enable Top Swap mode. PCH internal pull-down is disabled after PLTRST# deasserts.
LPSS_GSPI0_MOSI (GPP_B18/GSPI0_MOSI)	0: Disable No Reboot mode. 1: Enable No Reboot mode This function is useful when running ITP/XDP. The internal pull-down is disabled after PLTRST# deasserts.
PCH_PORT80_LED (GPP_C2/SMBALERT#)	0: Disable TSL confidentiality 1: Enable TSL confidentiality (default) The internal pull-down is disabled after RSMRST# deasserts.
LPSS_GSPI1_MOSI (GPP_B22/GSPI1_MOSI)	BOOT_SELECT_STRAP 0: SPI select 1: LPC select The internal pull-down is disabled after PLTRST# deasserts.
GPP_C_5 (GPP_C5/SML0ALERT#)	ESPI/LPC_SELECT_STRAP 0: LPC is selected for EC. 1: eSPI is selected for EC. The internal pull-down is disabled after RSMRST# deasserts.
PCH_HOT_R_N (GPP_B23/SML1ALERT#/PCHHOT#)	0: Disable Exi boot stall bypass 1: Enable Exi boot stall bypass The internal PD resistor is disable after RSMRST# de-asserted.
GPP_H_12 (GPP_H12/SML2ALERT#)	ESPI flash sharing mode 0: Master attached flash sharing 1: Slave attached flash sharing PCH has internal weak PD.
VISACH2_D3 (GPP_E12)	DFX test mode 0: XTAL input is single ended. 1: XTAL input is differential. The internal PD resistoris disabled after RSMRST# de-asserts
HDA_SDOUT_PCH (HDA_SDO)	0: Enable security measures defined in the Flash Descriptor. 1: Disable Flash Descriptor Security (override). The internal pull-down is disabled after PLTRST# deasserts.
SUSCLK_PCH (GPD8/SUSCLK)	0: Disable OD PLL VR 1: Enable OD PLL VR

Need check
Though CRB use LPC to connect EC.
This pin doen't pull down

Follow ROSA / D7 trigerfish & Lily / M800 skylake project.

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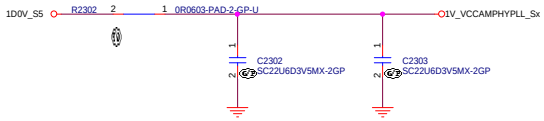
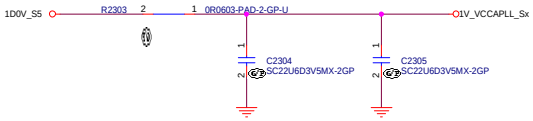
<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

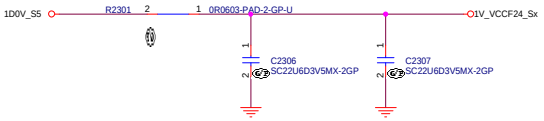
Title: PCH_(POWER2)
Size: C
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 22 of 107



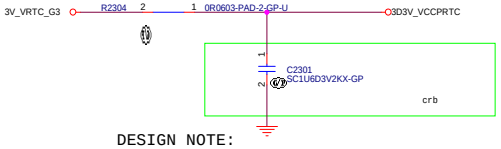
DESIGN NOTE:
PLACE HOLDER FOR VCCMPHYPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN A42,A43, AND B43



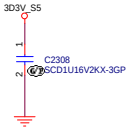
DESIGN NOTE:
PLACE HOLDER FOR VCCAUSB_1P0 AND VCCAAZPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN AJ5,AL5, AND AN19



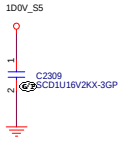
DESIGN NOTE:
PLACE HOLDER FOR VCCF24_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN K2 AND K3



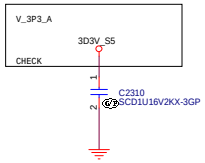
DESIGN NOTE:
BOARD CAP FOR VCCPRTC_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA22



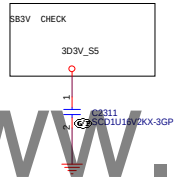
DESIGN NOTE:
EDGE CAP FOR VCCPGPPEF(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AJ41 AND AL41



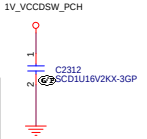
DESIGN NOTE:
BOAED CAP FOR VCCMPHY_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26



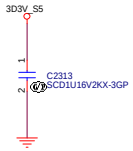
DESIGN NOTE:
EDGE CAP FOR VCCPUSBDSW_3P3
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
 PIN W15



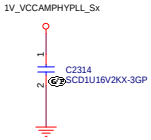
DESIGN NOTE:
BOAED CAP FOR VCCPRTCPRIM_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA20



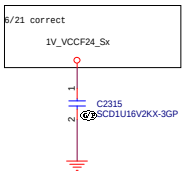
DESIGN NOTE:
BOAED CAP FOR VCCDSW_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA29



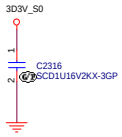
DESIGN NOTE:
EDGE CAP FOR VCCPGPPG(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AD41



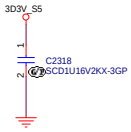
DESIGN NOTE:
BOAED CAP FOR VCCMPHYPLL_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN A42,A43 AND B43



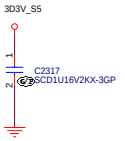
DESIGN NOTE:
BOAED CAP FOR VCCF24_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN K2,K3



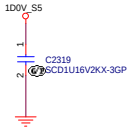
DESIGN NOTE:
BOAED CAP FOR VCCATS
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN AD13



DESIGN NOTE:
EDGE CAP FOR VCCPGPPBCH(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN BC42 AND BD40



DESIGN NOTE:
BOAED CAP FOR VCCPHVC_3P3(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AN15



DESIGN NOTE:
EDGE CAP FOR VCCMPHY_1P0 AND VCCDUSB_1P0
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26,AND AC17

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<Core Design>

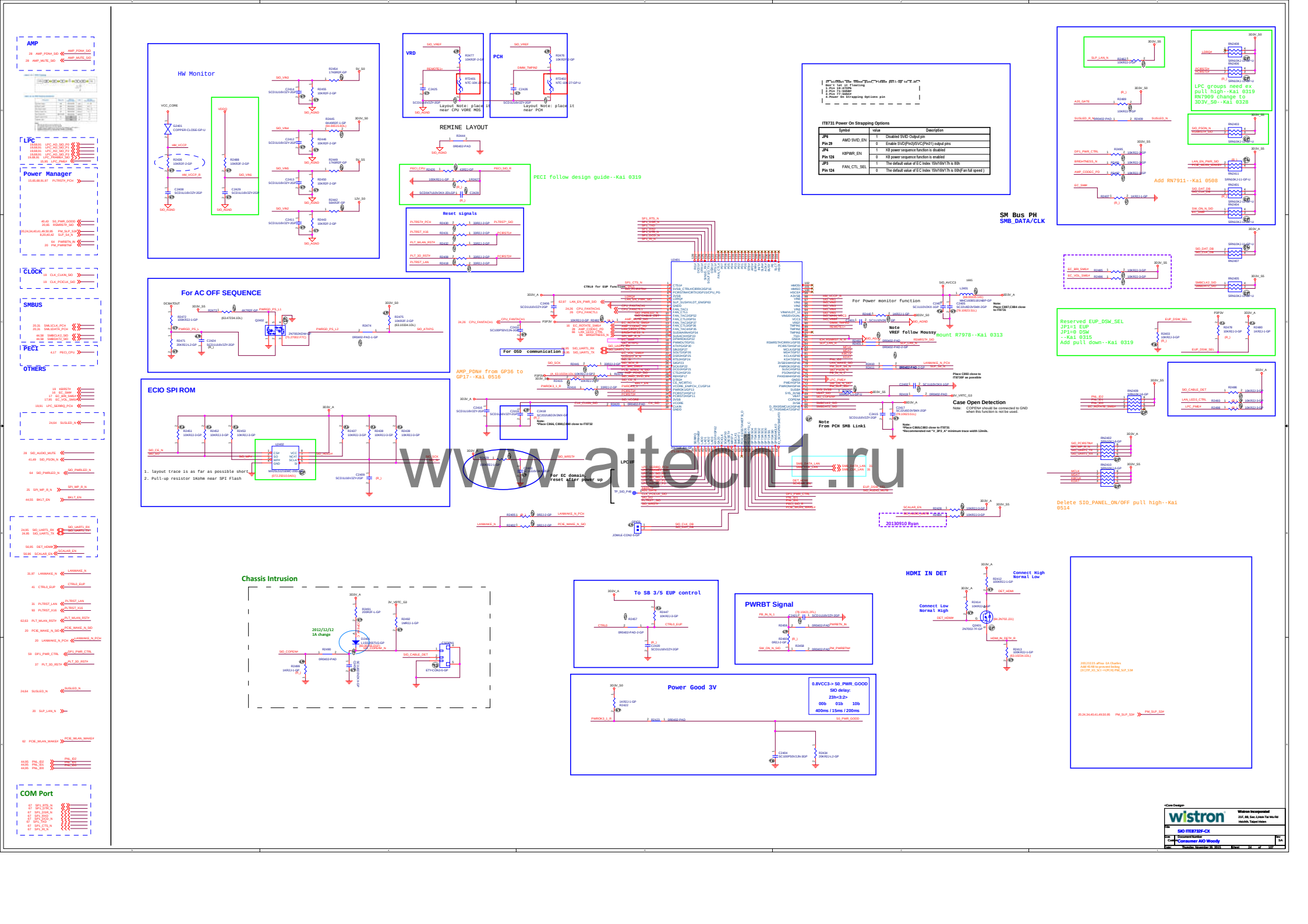
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH Power CAP

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 23 of 107



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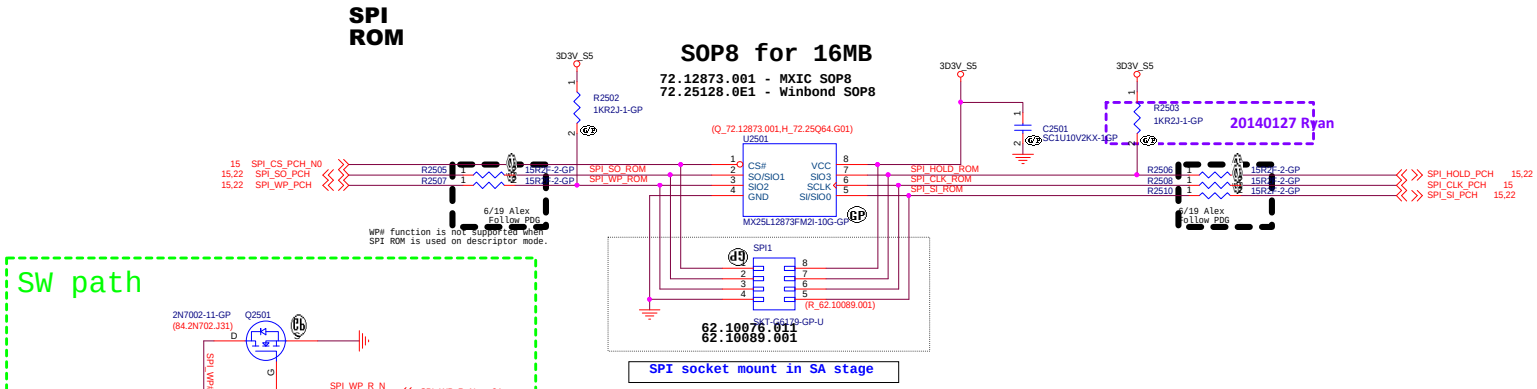
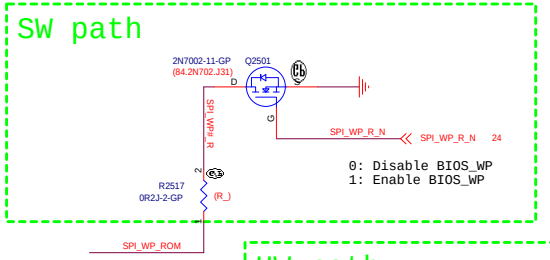
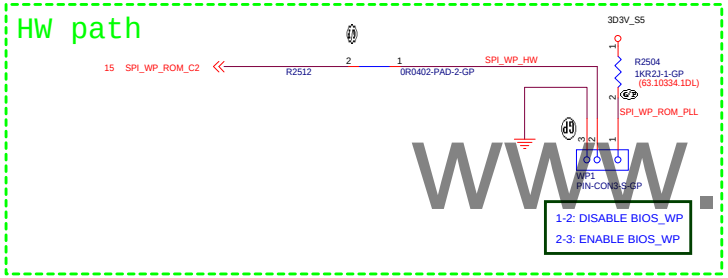
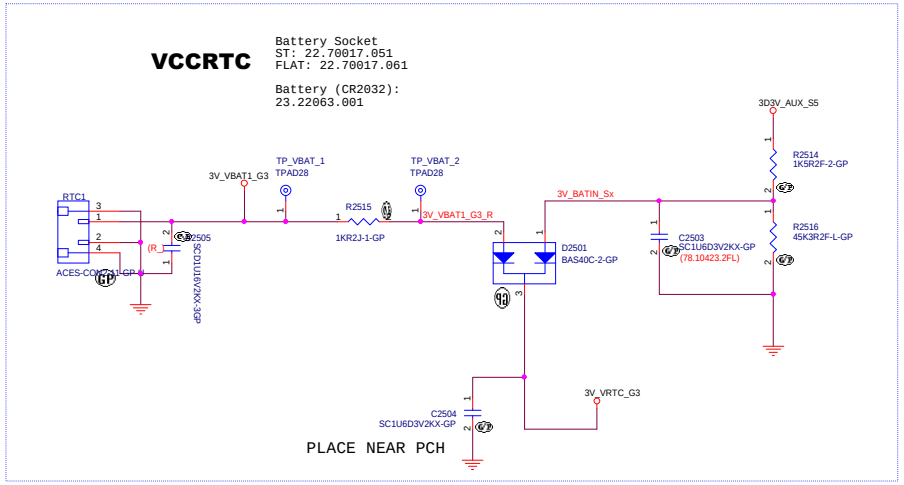




2014/8/6
add SPI1 62.10076.011

Single Flash Device: 15ohom
Dual Flash Device: 33ohm





SKL Platforms – SPI0_IO3 Signal Implementation Requirement for ES or pre-ES1/ES1 Samples

An Intel internal debug strap is implemented on the SPI0_IO3 signal. However, the strap is not functioning as expected on ES (SKL U/Y platform) and pre-ES1/ES1 (SKL S/H platform) samples and could prevent the system from booting. The issue will be fixed in future samples.

To ensure the platform boots with these early samples, Intel recommends customers to implement a pull-down resistor on the SPI0_IO3 signal aside from the 1 kOhm pull-up resistor which is already a requirement on the signal. There are two options to implement the pull-down resistor:

Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Option 2: Implement a strong pull-down resistor (e.g. 100 Ohm) on the signal and disable it after RSMRST# de-assertion.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

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wistron

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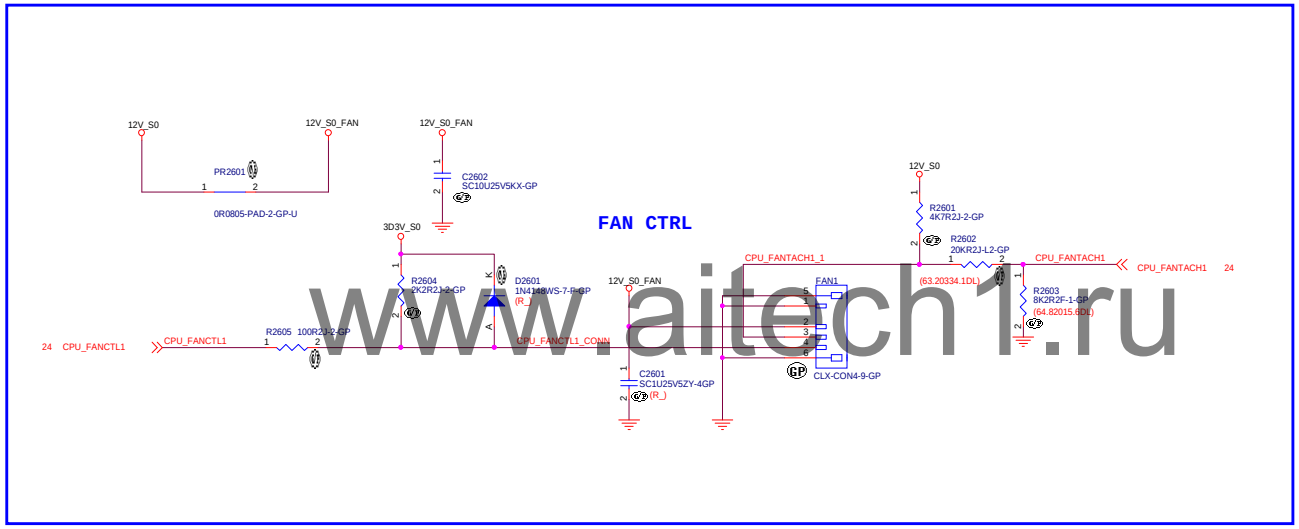
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Flash&RTC
Size: C
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
Sheet 25 of 107



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<Core Design>

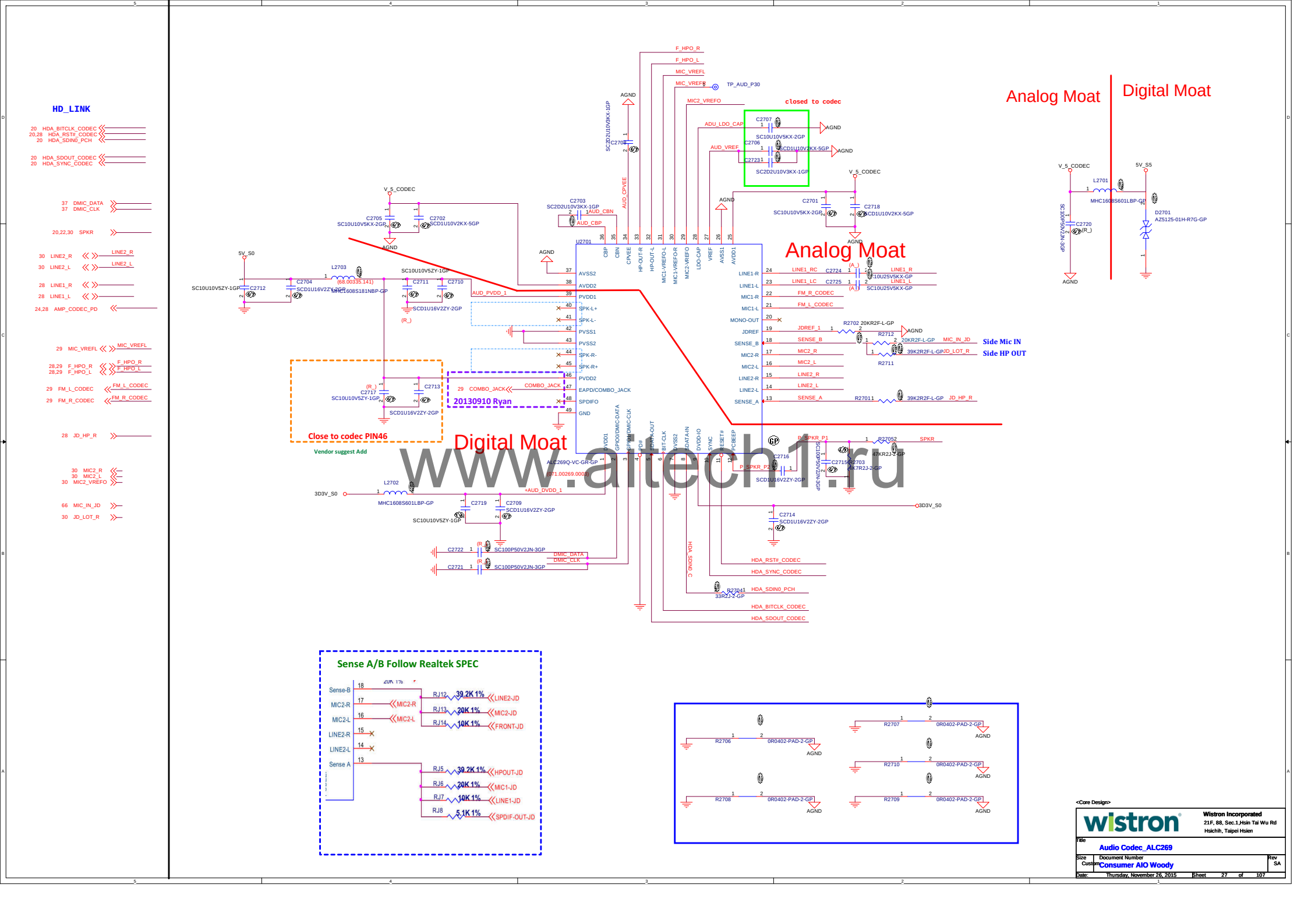
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Thermal & FAN

Size	Document Number	Rev
C	Consumer AIO Woody	SA

Date: Thursday, November 26, 2015 Sheet 26 of 107


HD_LINK
20 HDA_BITCLK_CODEC
20,28 HDA_RST#_CODEC
20 HDA_SDIN0_PCH
20 HDA_SDOUT_CODEC
20 HDA_SYNC_CODEC
37 DMIC_DATA
37 DMIC_CLK
20,22,30 SPKR
30 LINE2_R
30 LINE2_L
28 LINE1_R
28 LINE1_L
24,28 AMP_CODEC_PD
29 MIC_VREFL
28,29 F_HPO_R
28,29 F_HPO_L
29 FM_L_CODEC
29 FM_R_CODEC
28 JD_HP_R
30 MIC2_R
30 MIC2_L
30 MIC2_VREFO
66 MIC_IN_JD
30 JD_LOT_R
Analog Moat
Digital Moat
Analog Moat
Digital Moat
closed to codec
Side Mic IN
Side HP OUT
20130910 Ryan
Close to codec PIN46
Vendor suggest Add
Sense A/B Follow Realtek SPEC
www.altech1.ru
<Core Design>
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Audio Codec_ALC269
Consumer AIO Woody
Thursday, November 26, 2015
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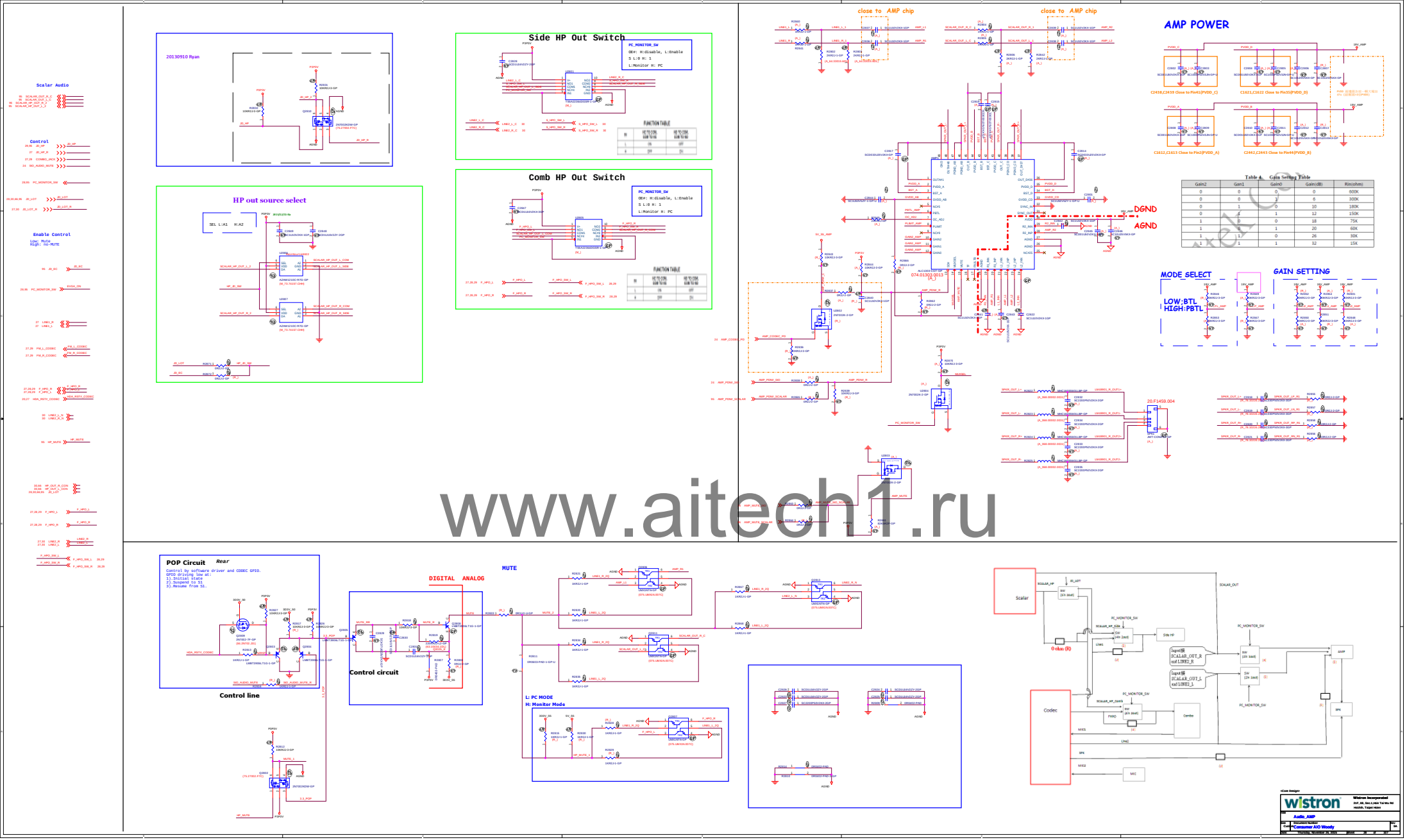
107



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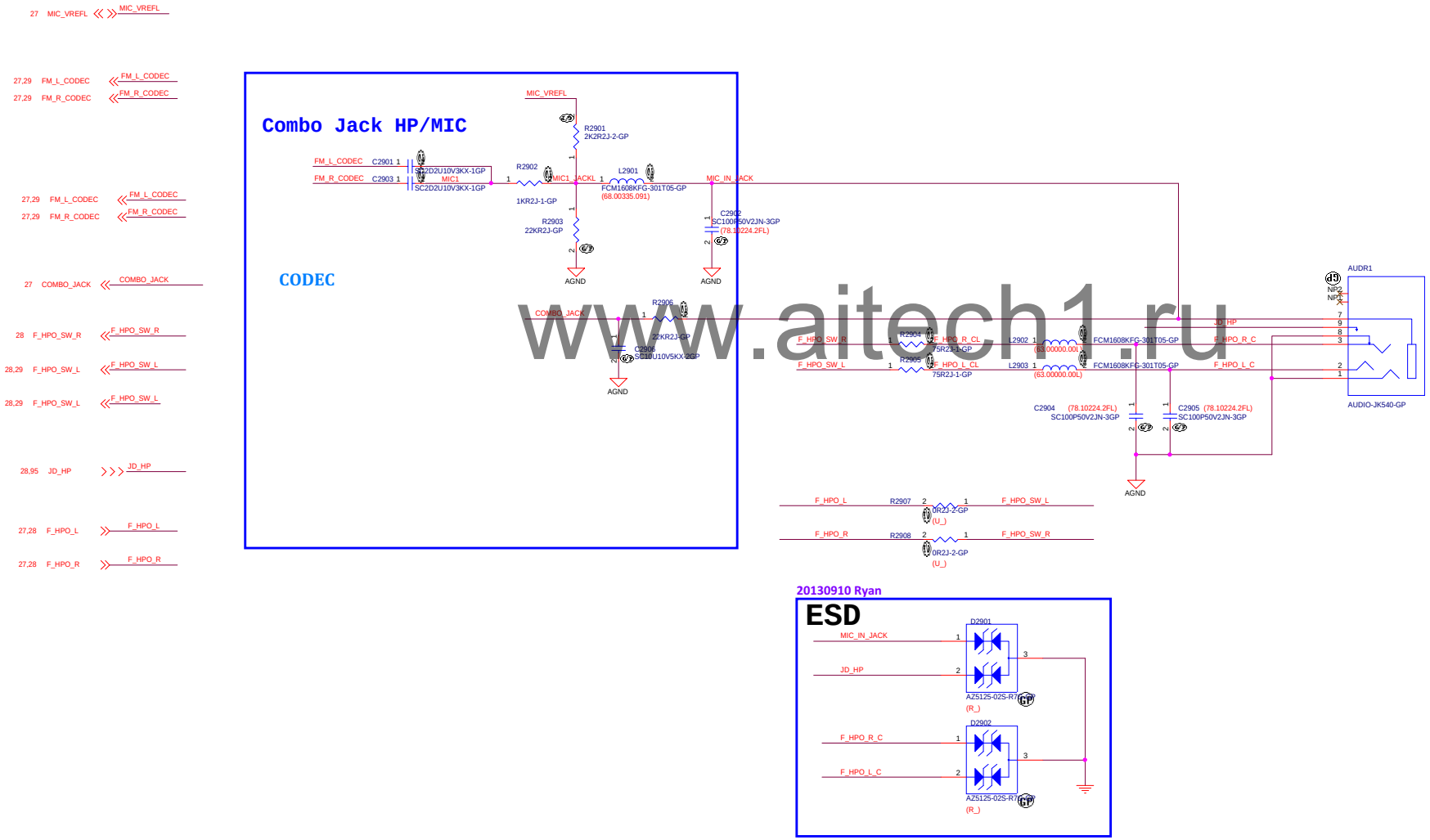

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<Core Design>

wistron

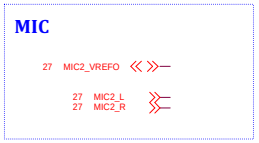
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

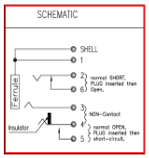
Title: Audio IO_Combo HP_MIC

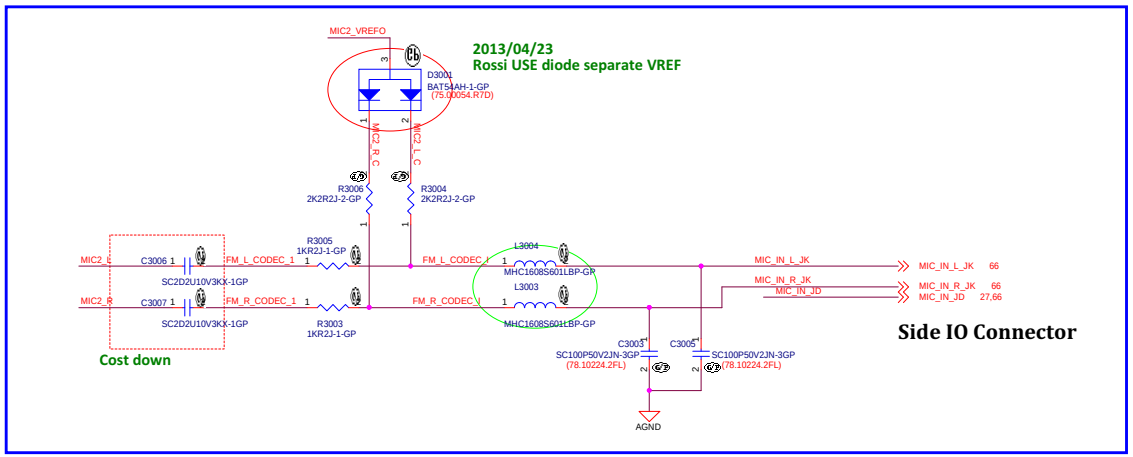
Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 29 of 107

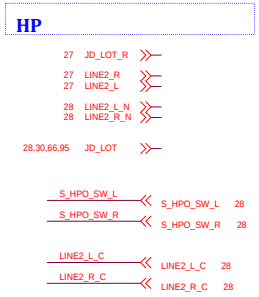
MIC

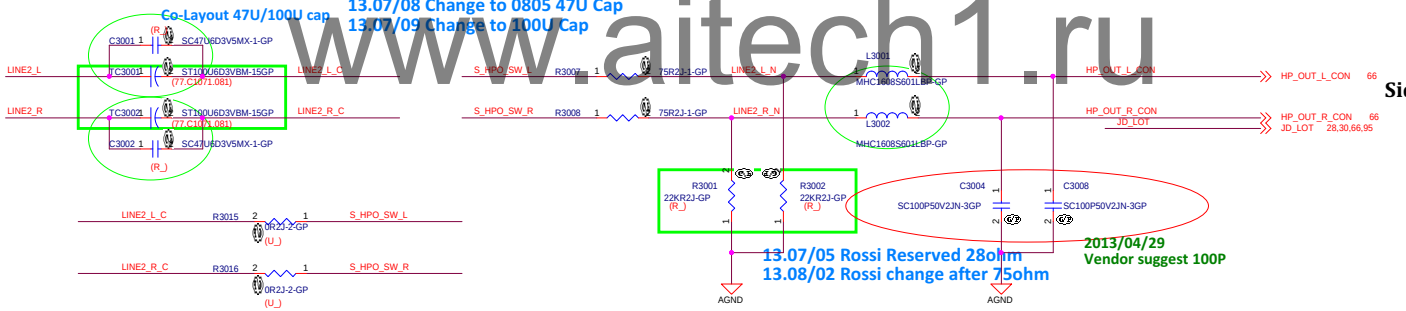






HP





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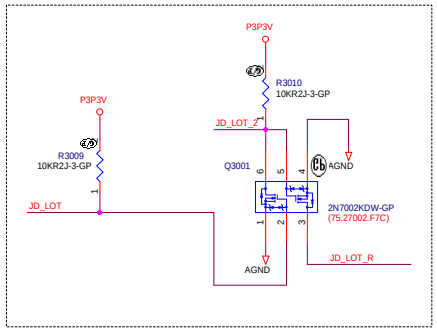

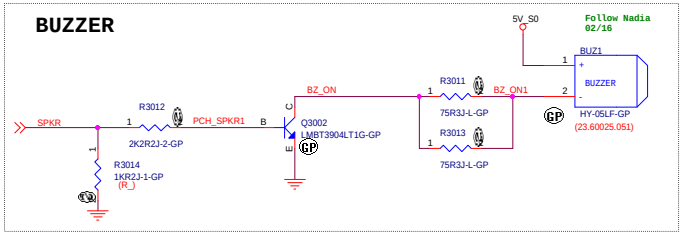

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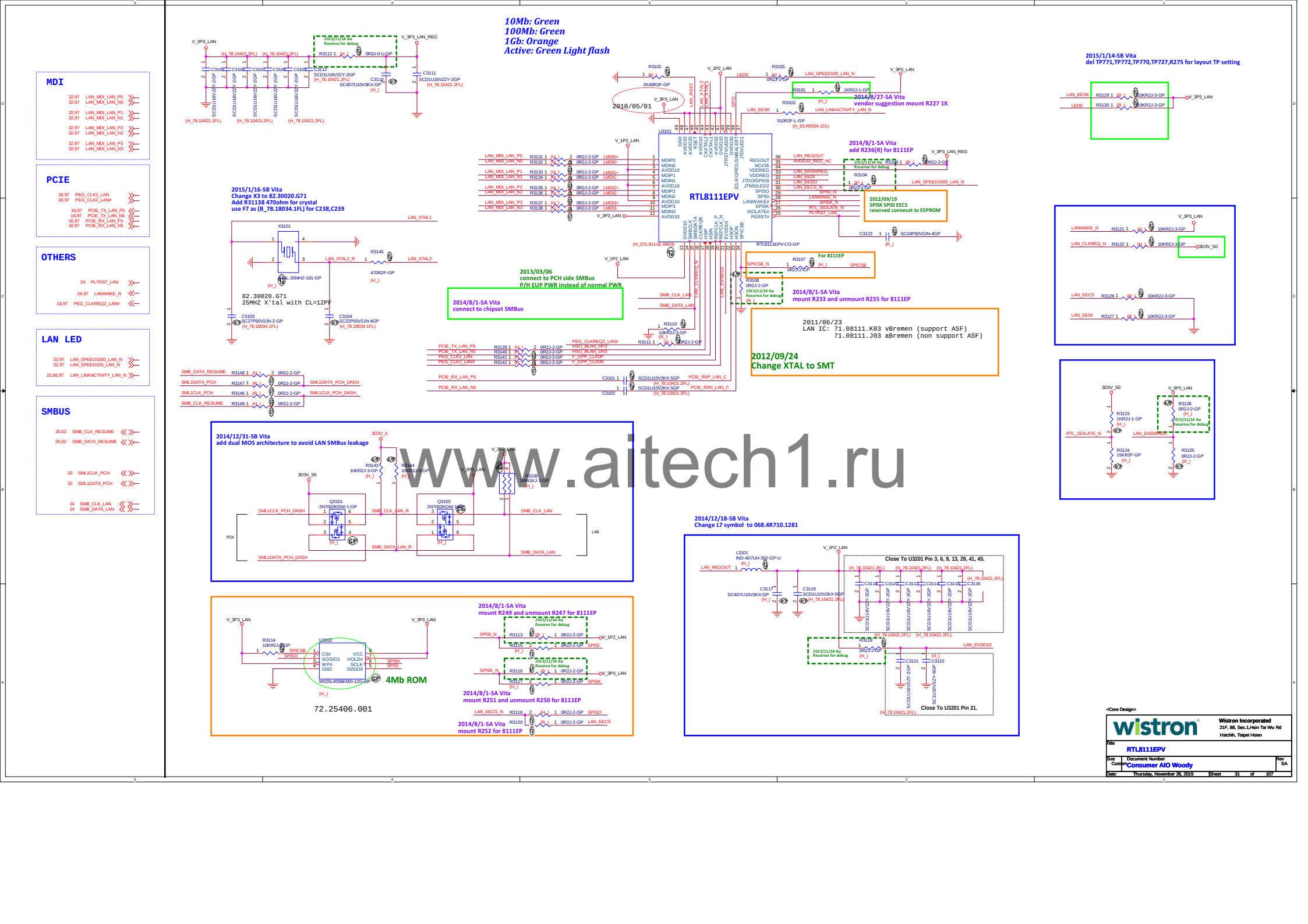
Hsichih, Taipei Hsien

Title: Audio IO_Side

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 30 of 107


MDI
PCIE
OTHERS
LAN LED
SMBUS
10Mb: Green
100Mb: Green
1Gb: Orange
Active: Green Light flash
RTL8111EPV
2015/1/16-SB Vita
Change X3 to 82.30020.G71
Add R3138 470ohm for crystal
use F7 as (B_78.18034.1FL) for C238,C239
82.30020.G71
25MHZ X'tal with CL=12PF
2014/8/1-SA Vita
connect to chipset SMBus
2013/03/06
connect to PCH side SMBus
P/H EUP PWR instead of normal PWR
2014/8/1-SA Vita
add R236(R) for 8111EP
2012/09/19
SPISK SPISI EECS
reserved connecot to EEPROM
2014/8/1-SA Vita
mount R233 and unmount R235 for 8111EP
2011/06/23
LAN IC: 71.08111.K03 vBremen (support ASF)
71.08111.J03 aBremen (non support ASF)
2012/09/24
Change XTAL to SMT
2014/8/27-SA Vita
vendor suggestion mount R227 1K
2015/1/14-SB Vita
del TP771,TP772,TP770,TP727,R275 for layout TP setting
2014/12/31-SB Vita
add dual MOS architecture to avoid LAN SMBus leakage
2014/12/18-SB Vita
Change L7 symbol to 068.4R710.1281
Close To U3201 Pin 3, 6, 9, 13, 29, 41, 45.
Close To U3201 Pin 21.
2014/8/1-SA Vita
mount R249 and unmount R247 for 8111EP
2014/8/1-SA Vita
mount R251 and unmount R250 for 8111EP
2014/8/1-SA Vita
mount R252 for 8111EP
4Mb ROM
72.25406.001
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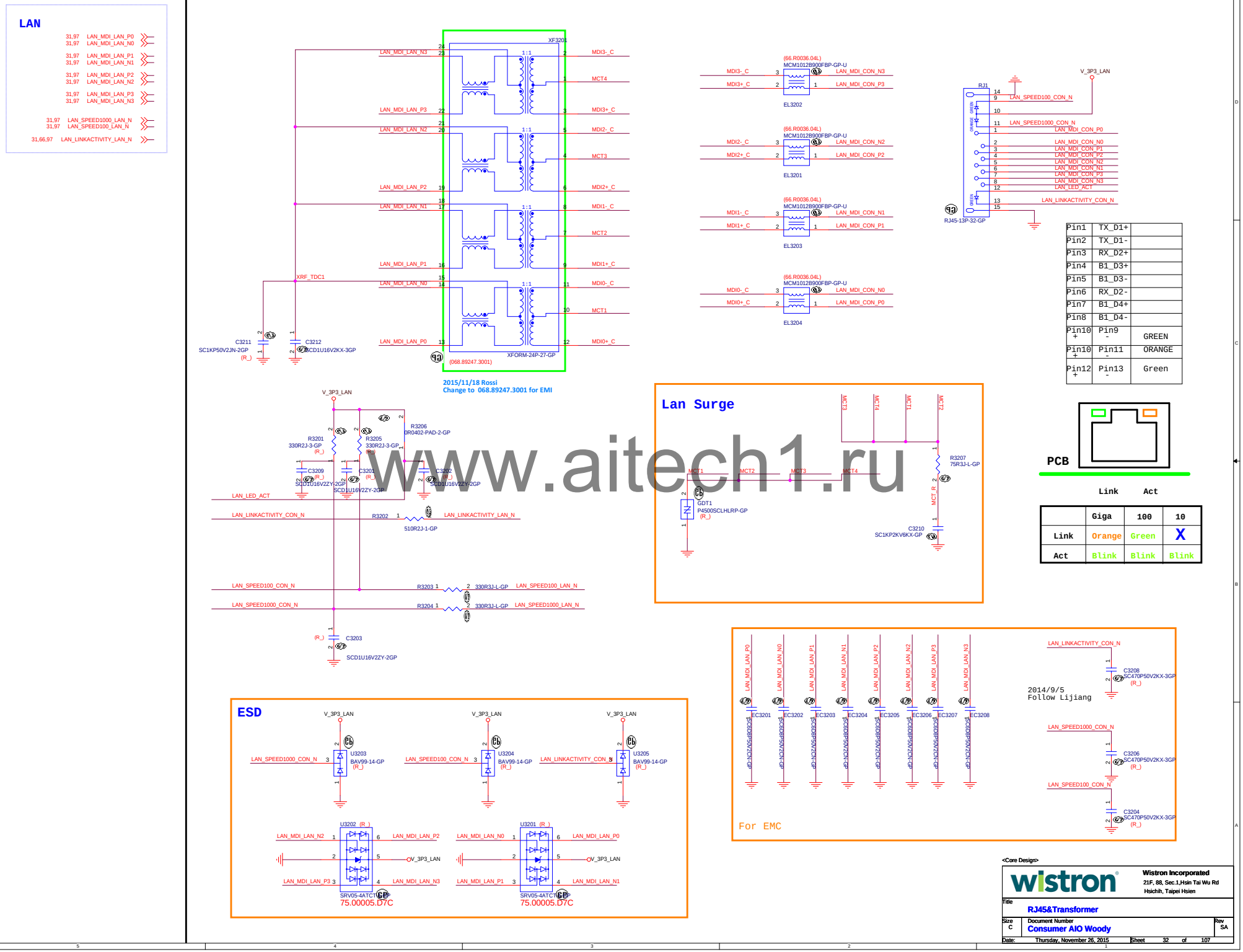
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
RTL8111EPV
Consumer AIO Woody
Thursday, November 26, 2015



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Title: Card reader_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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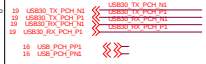
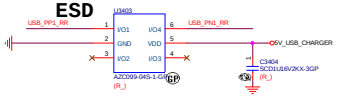
USB3.0 SIDE CONNECTOR

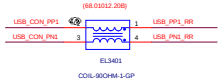


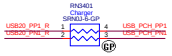
USB3.0's USB2 pair from PCH

ESD

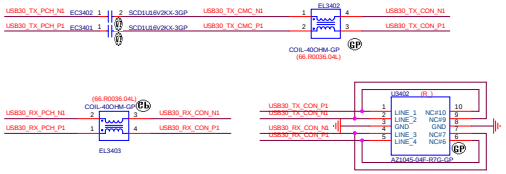


USB2.0 EMI

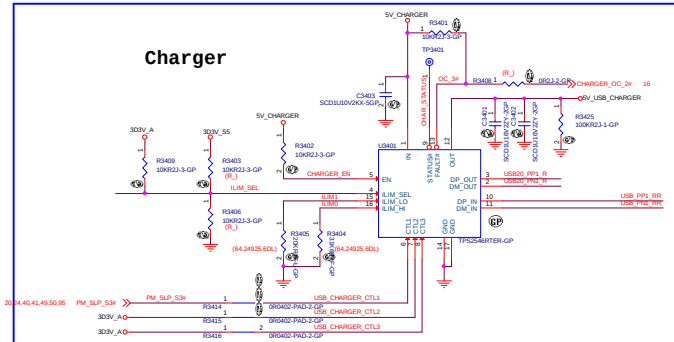




USB3.0 EMI



Charger



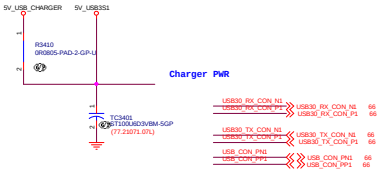
Truth Table for TPS2540A/TPS2543/TPS2546

ACPI Control	CTL1	CTL2	CTL3	ILIM_SEL	PWR	Control Mode
S0	1	1	1	1	+5V_MAIN	CDP
S1	1	1	1	1	+5V_MAIN	CDP
S3	0	1	1	1	ATX_5VSB	DCP
S4	0	1	1	1	ATX_5VSB	DCP
S5	0	1	1	1	ATX_5VSB	DCP
S5_EuP	0	1	1	1	ATX_5VSB	DCP
G3->S5	0	1	1	1	ATX_5VSB	DCP

Paid attantion to CTRL1 and CTRL3 GPIO pin selection

	CTRL1	CTRL2	CTRL3	ILIM_SEL
S0	High	High	High	High
S3	Low	High	High	High
S4	Low	High	High	High
S5	Low	High	High	High

Side IO BD



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

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Title: USB Charger_TPS2544

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Title: USB_Redrive_(R)

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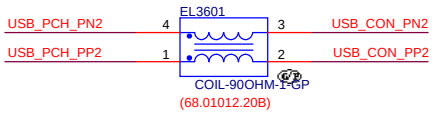
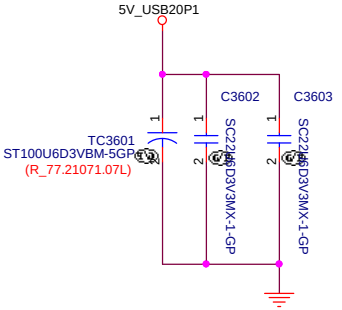
16 USB_PCH_PN2
16 USB_PCH_PP2

USB2.0 EMI





USB30_RX_CON_N2 → USB30_RX_CON_N2 38
USB30_RX_CON_P2 → USB30_RX_CON_P2 38
USB30_TX_CON_N2 → USB30_TX_CON_N2 38
USB30_TX_CON_P2 → USB30_TX_CON_P2 38
USB_CON_PN2 → USB_CON_PN2 38
USB_CON_PP2 → USB_CON_PP2 38

19 USB30_TX_PCH_N2
19 USB30_TX_PCH_P2
19 USB30_RX_PCH_N2
19 USB30_RX_PCH_P2

USB3.0 EMI

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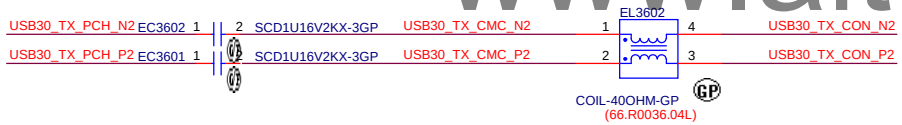

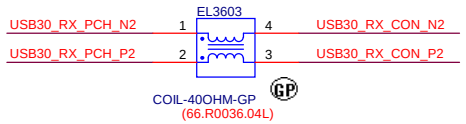

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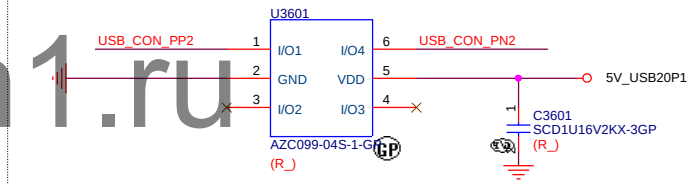

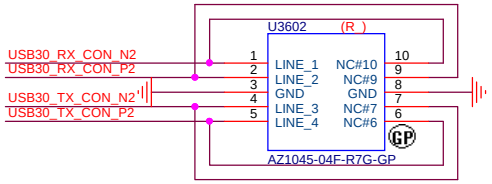

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Title: USB 30_REAR PORT

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

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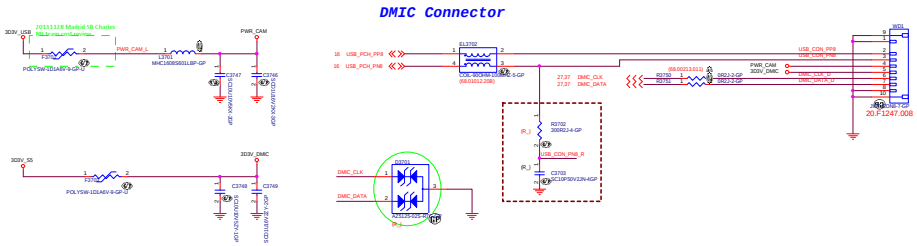
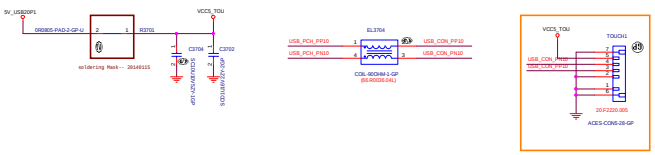
USB Port8 -> WEBCAM

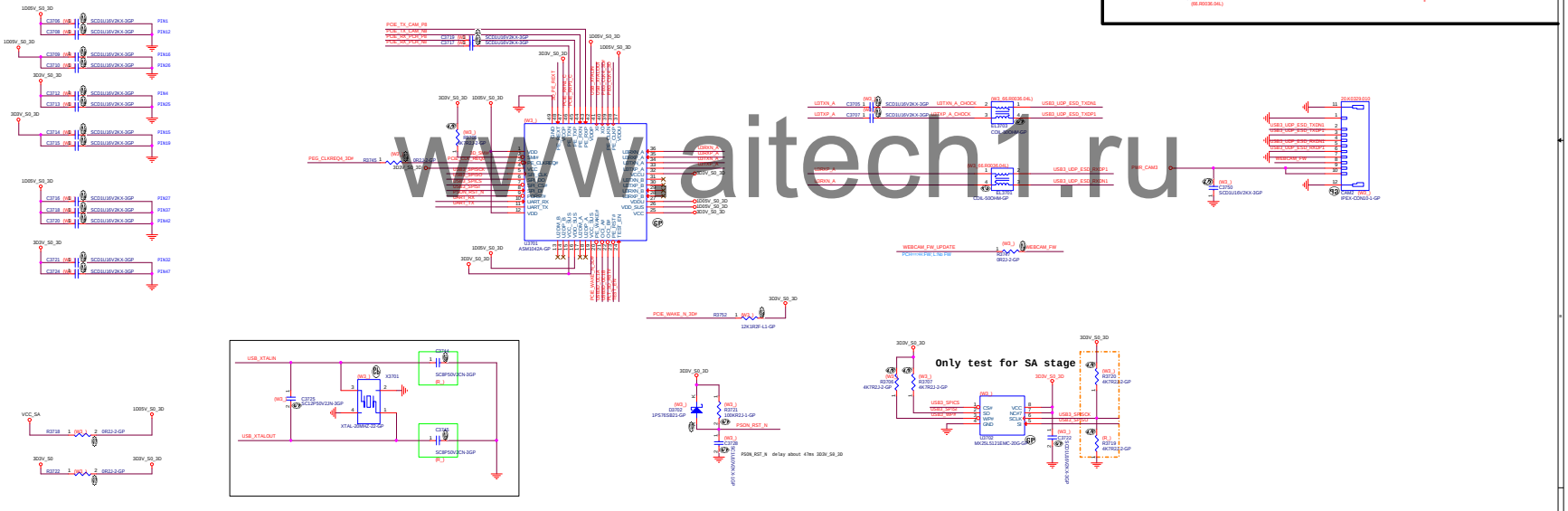


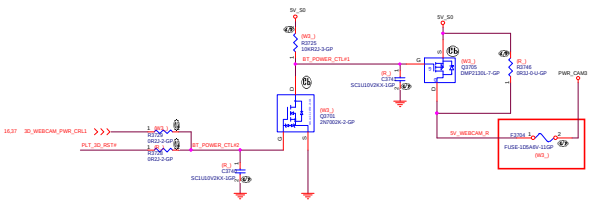
USB Port7 -> Touch

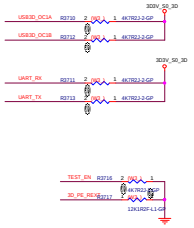


PCIE1->3D WEBCAM

09/06/2015 Add Internal USB connector
power use rear USB2.0 power







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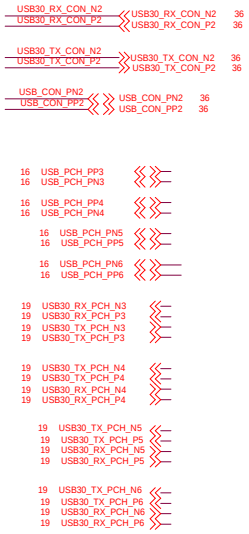
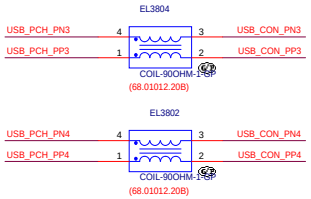
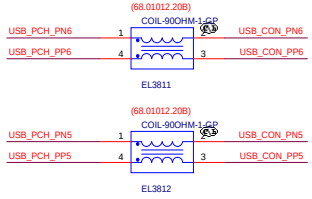


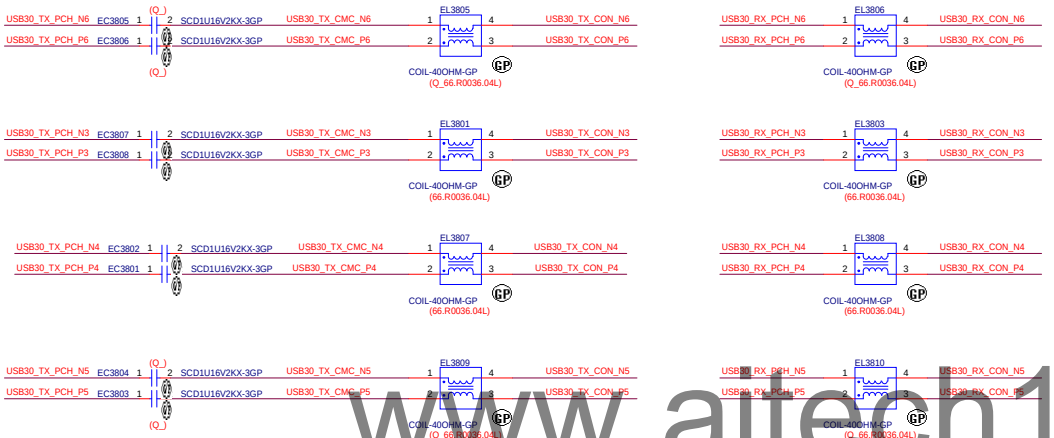
USB2.0 EMI



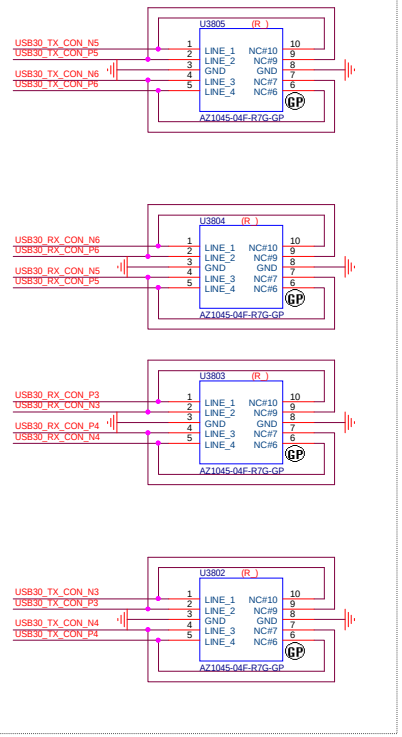
USB2.0 EMI



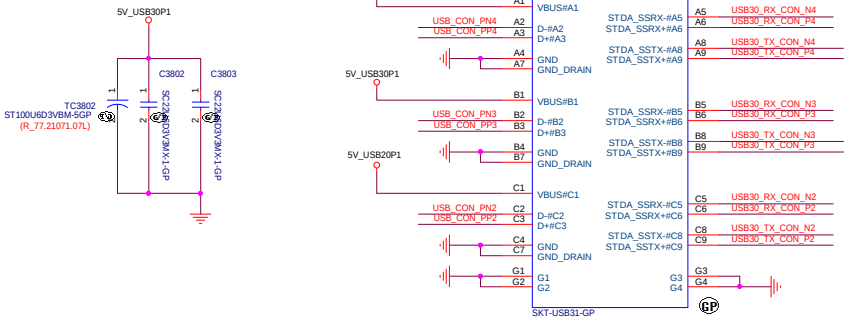
USB3.0 EMI



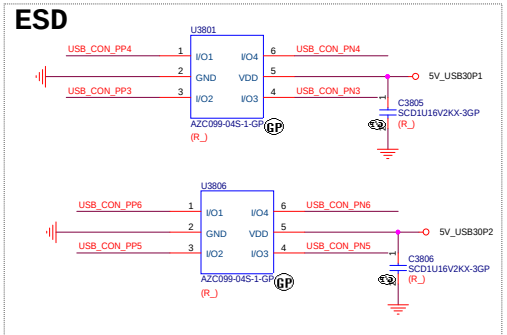
ESD



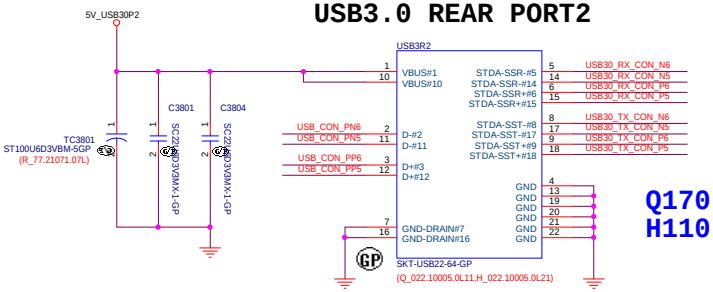
USB3.0 REAR PORT1



ESD



USB3.0 REAR PORT2



Q170:(USB 3.0*4)
H110:(USB3.0*2, USB2.0*2)

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Title: USB30_REAR PORT

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Title: USB30_(R)

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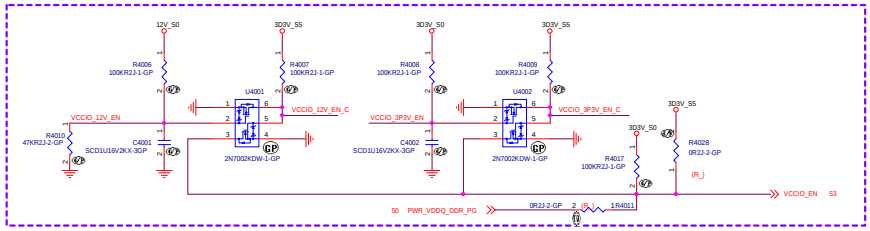
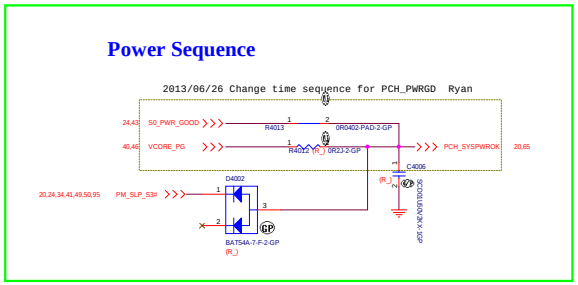
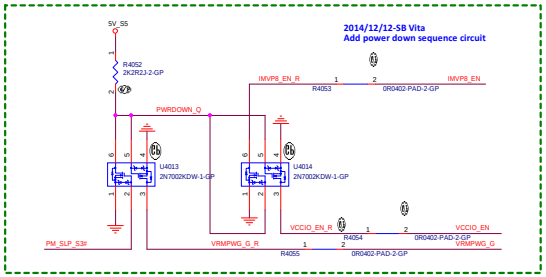
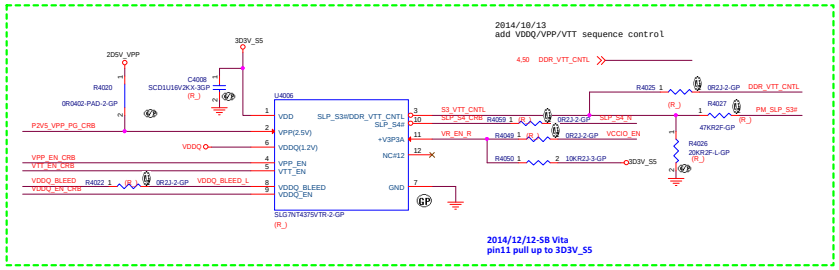
2014/9/23
VCCIO ENABLE
follow Yama D7



2014/8/7
follow Madrid

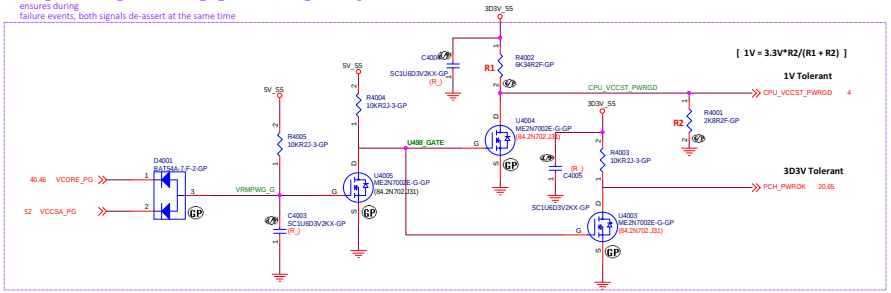


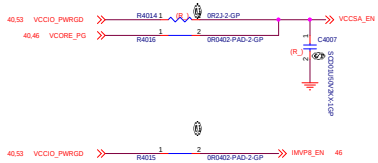




2014/8/7
Follow Veneno

Note:
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both
VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD and / or SLP_S3# in their generation. This ensures during
failure events, both signals de-assert at the same time





1> VCCIO -> VCORE -> VCCSA (current)
2> VCCIO -> VCORE/VCCSA both

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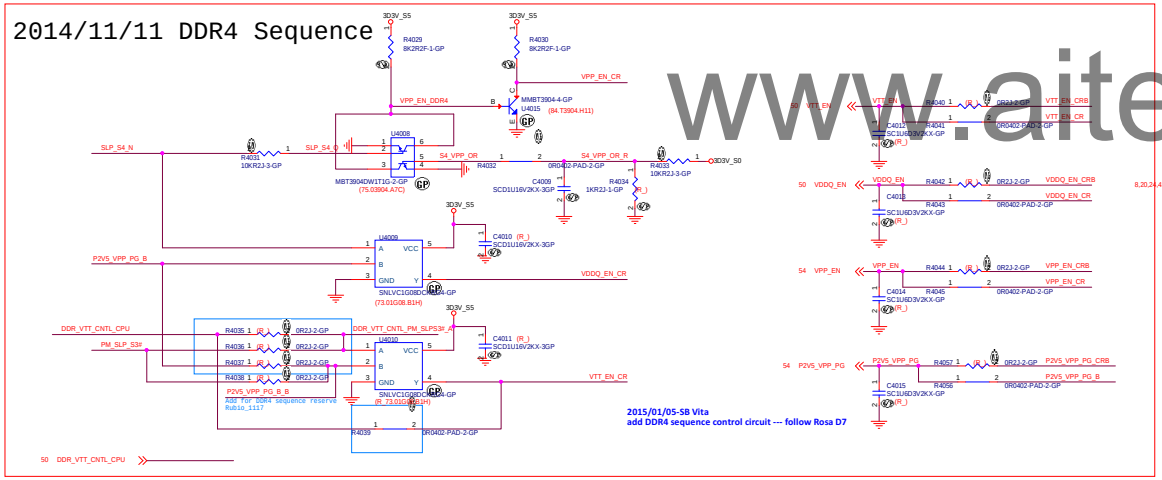
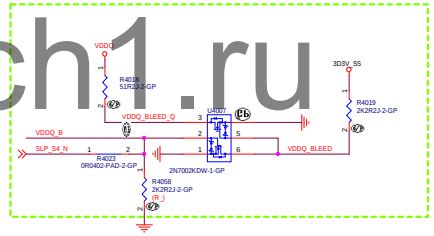
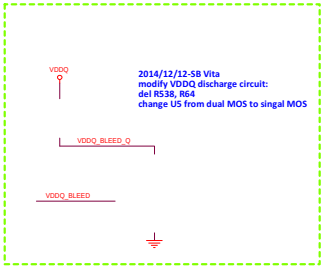
2014/11/11 DDR4 Sequence







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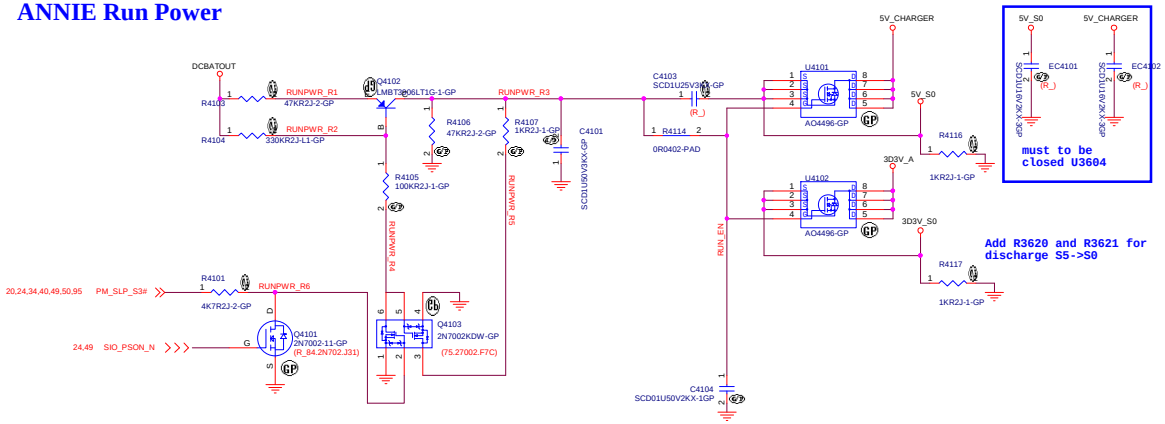
Title	Power Plane EN Sequence	
Size: Custom	Document Number: Consumer AIO Woody	Rev: SA
Date: Thursday, November 26, 2015	Sheet 40 of 107	

ANNIE Run Power



EUP Power

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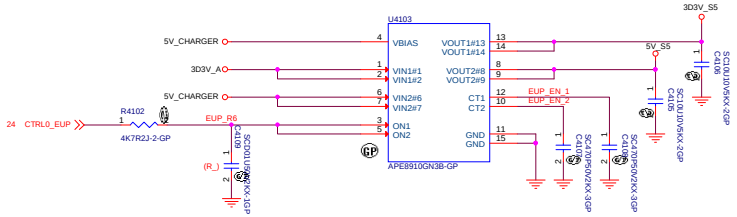
Modify 3V/5V Logic Control as Load Switch

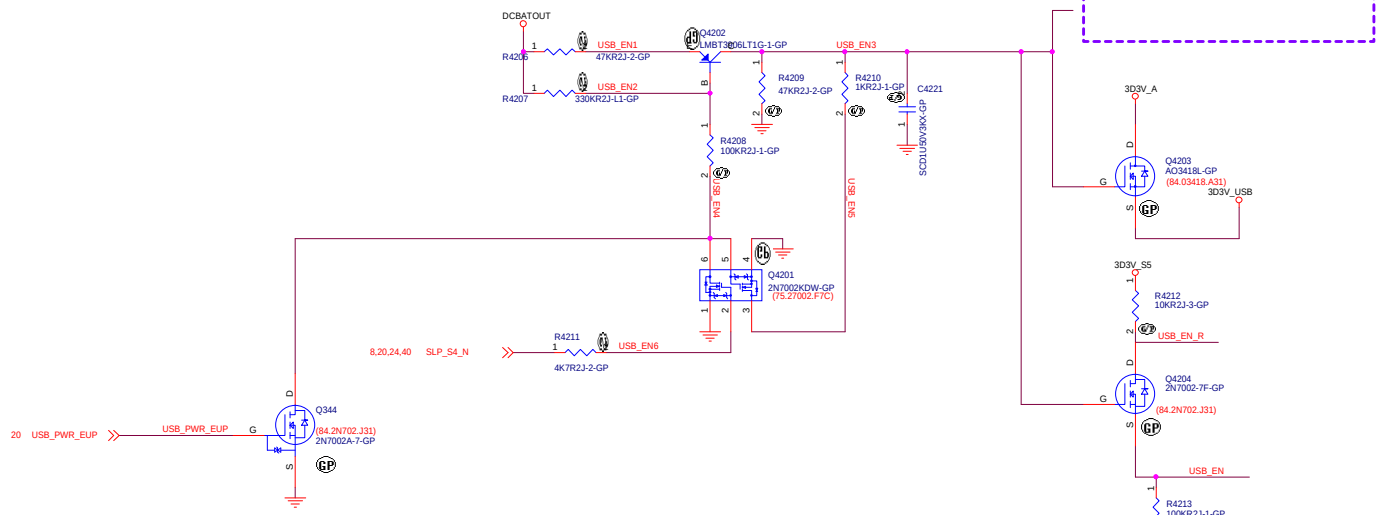


	S5	S4	S3-S0		S5	S4	S3-S0	Status
USB_PWR_SLP	L	L	L	USB_EN	L	L	H	No Support S4 USB wake up
USB_PWR_SLP	L	H	L	USB_EN	L	H	L	Support S4 USB wake up

S4, S5 --> choice by USB_PWR_SLP
S3-S0 --> choice by SLP_S4#

VCC5_USB

20130927 Ryan



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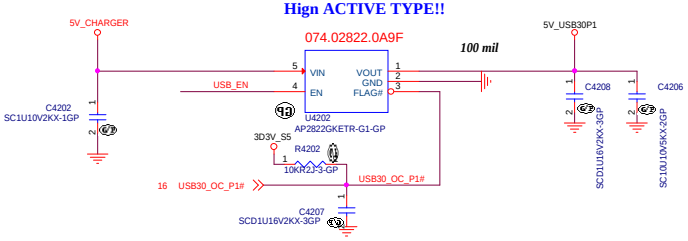
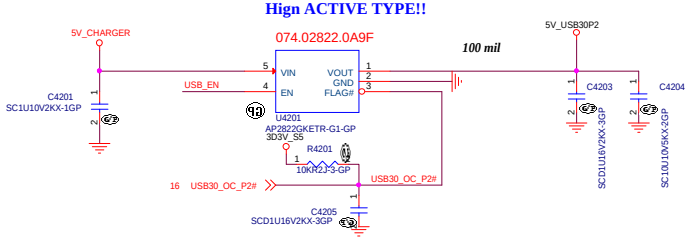
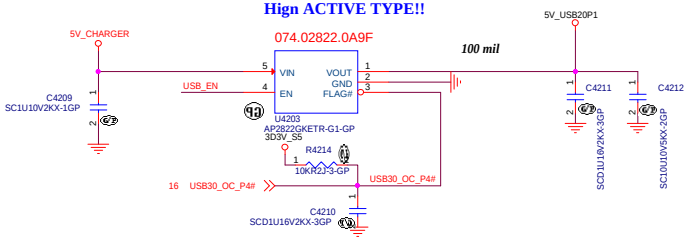
Hign ACTIVE TYPE!!



Hign ACTIVE TYPE!!



Hign ACTIVE TYPE!!



<Core Design>

Wistron Incorporated
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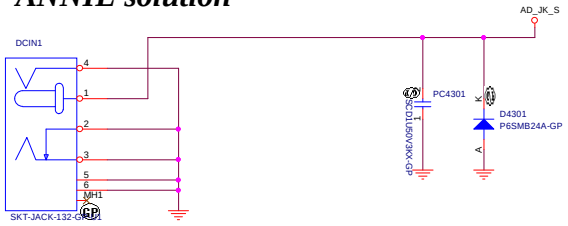
Hsichih, Taipei Hsien

Title: Switch power

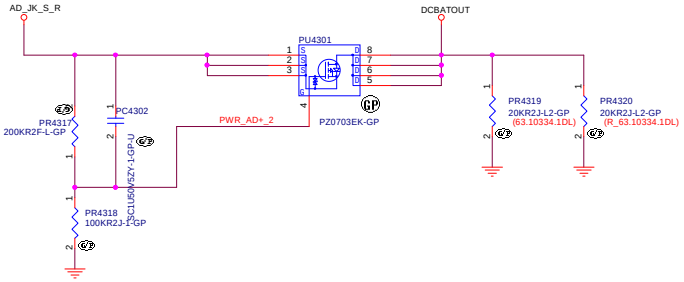
Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 42 of 107

ANNIE solution



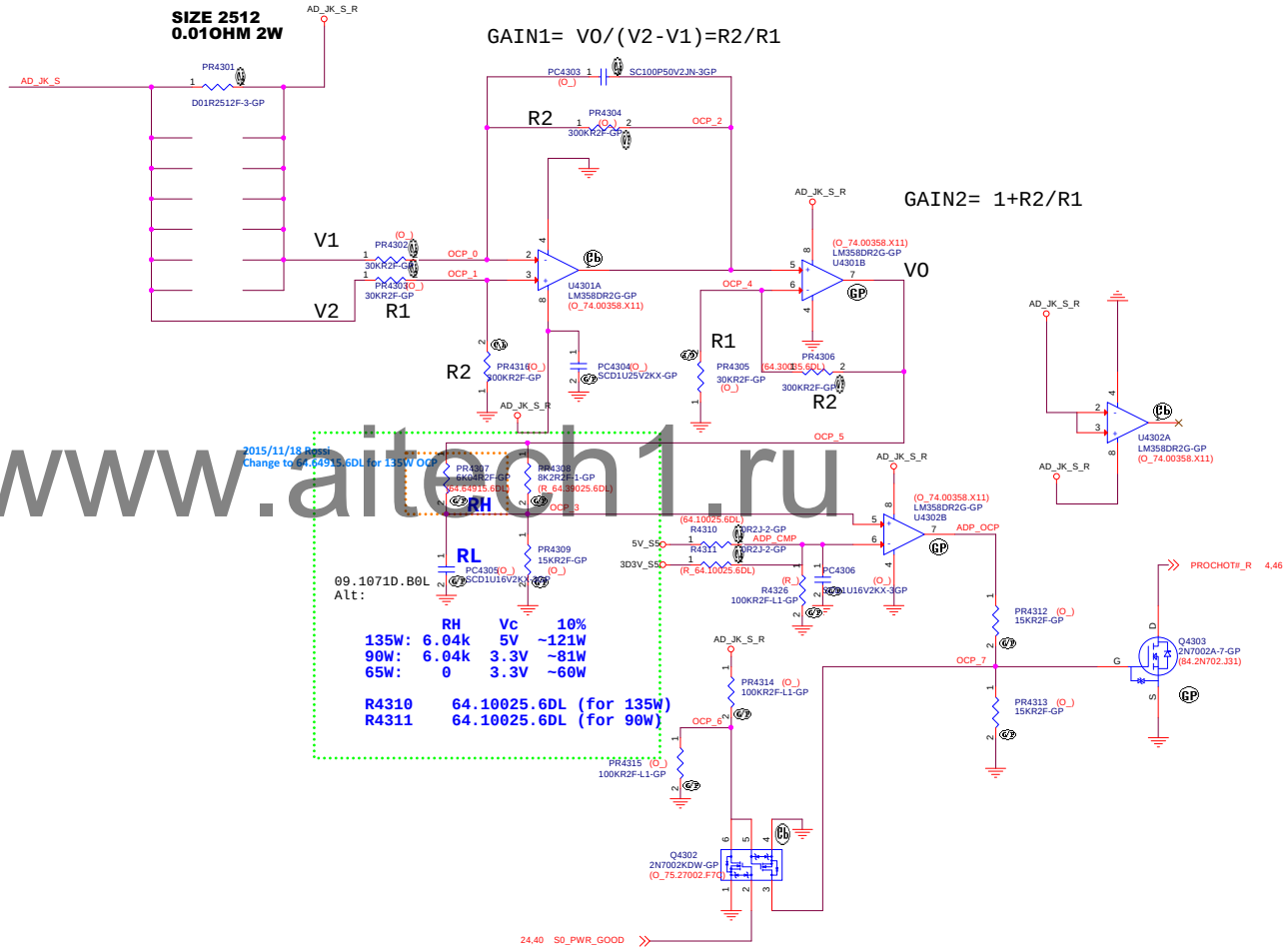
DCIN1 PN Change to 22.10037.A41



SIZE 2512
0.01OHM 2W

GAIN1= VO/(V2-V1)=R2/R1

GAIN2= 1+R2/R1



2015/11/18 Rose:
Change to 64.64915.6DL for 135W OCP

09.1071D.B0L
Alt:

	RH	Vc	10%
135W:	6.04k	5V	~121W
90W:	6.04k	3.3V	~81W
65W:	0	3.3V	~60W

R4310 64.10025.6DL (for 135W)
R4311 64.10025.6DL (for 90W)

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<Core Design>

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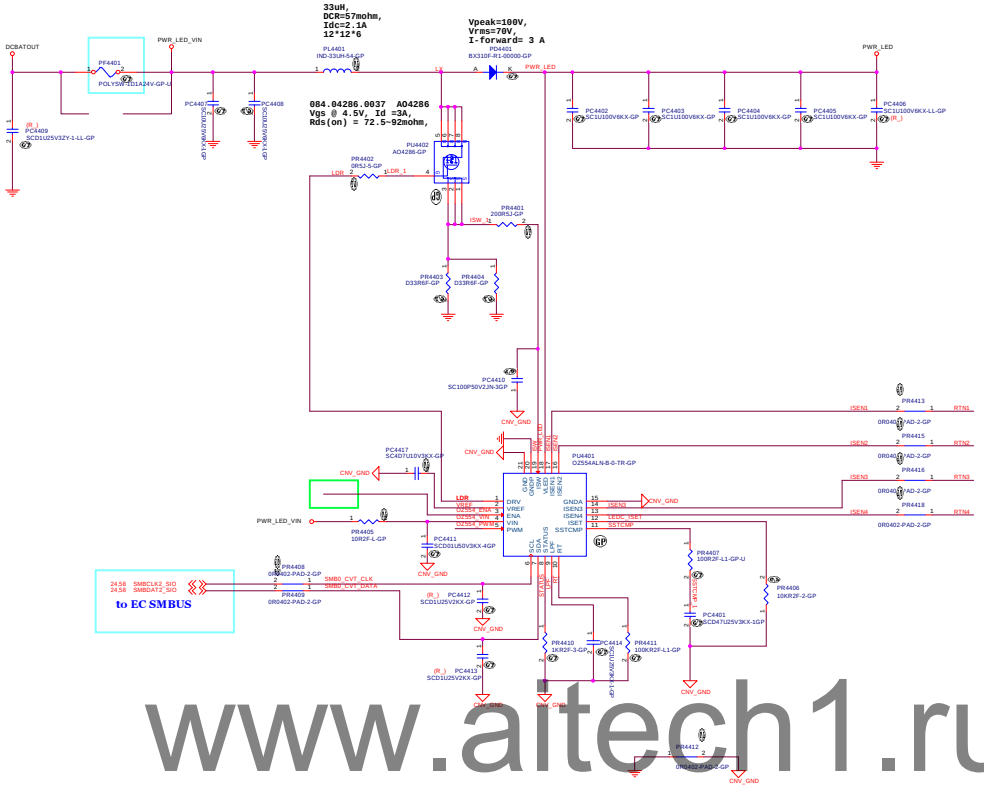
Title	DCIN JACK(BATT Conn)
Size: Custom	Document Number: Consumer AIO Woody
Rev	SA
Date: Thursday, November 26, 2015	Sheet 43 of 107

Converter Board

Cable detection			
PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Status
1	1	1	Panel unplug
X	X	X	Panel plug



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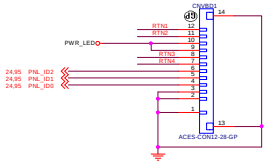
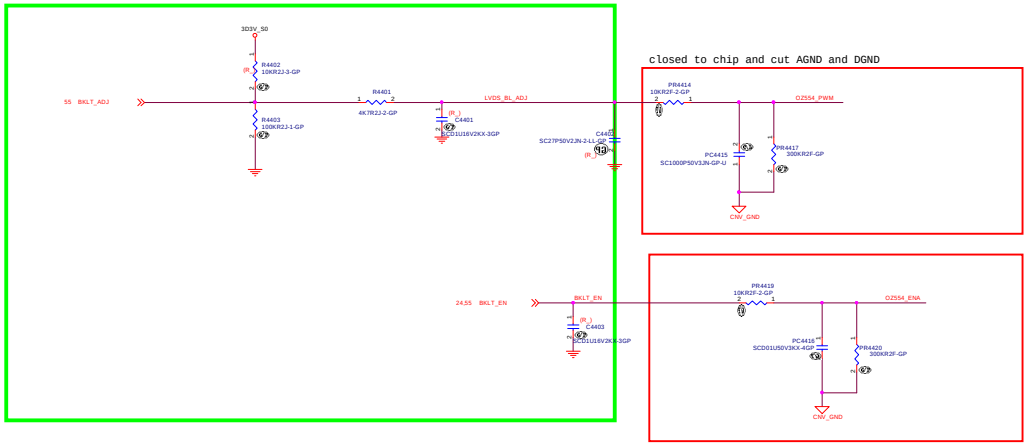
Follow Madrid



Need EE to check



Panel Model	Cable Spec			
	ID0	ID1	ID2	Vout
	0	0	0	
	0	0	1	
	0	1	0	
	1	0	0	
	1	1	0	
	1	1	1	

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: OZ554A LED Converter

Size: D | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 44 of 107

PWR_3D3V/PWR_5V

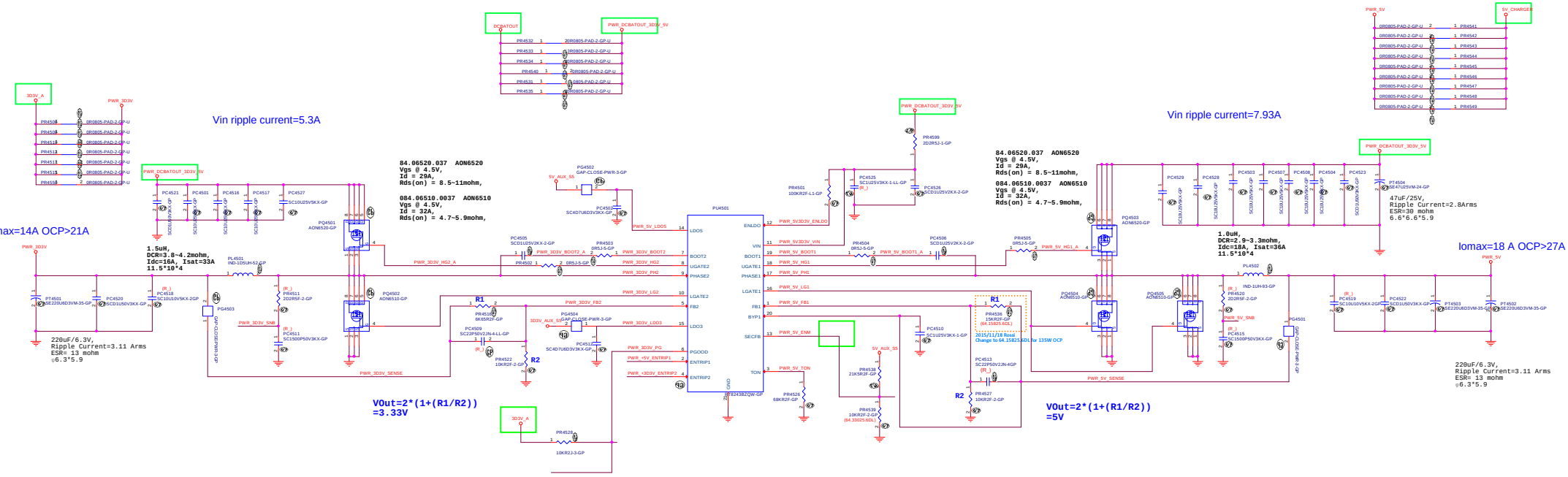


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Table 2. Power Up Sequencing(RT8243A)

ENLDO(V)	SECFB	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SMPS1	SMPS2
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On=>PD	On=>PD	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	On

<Core Design>
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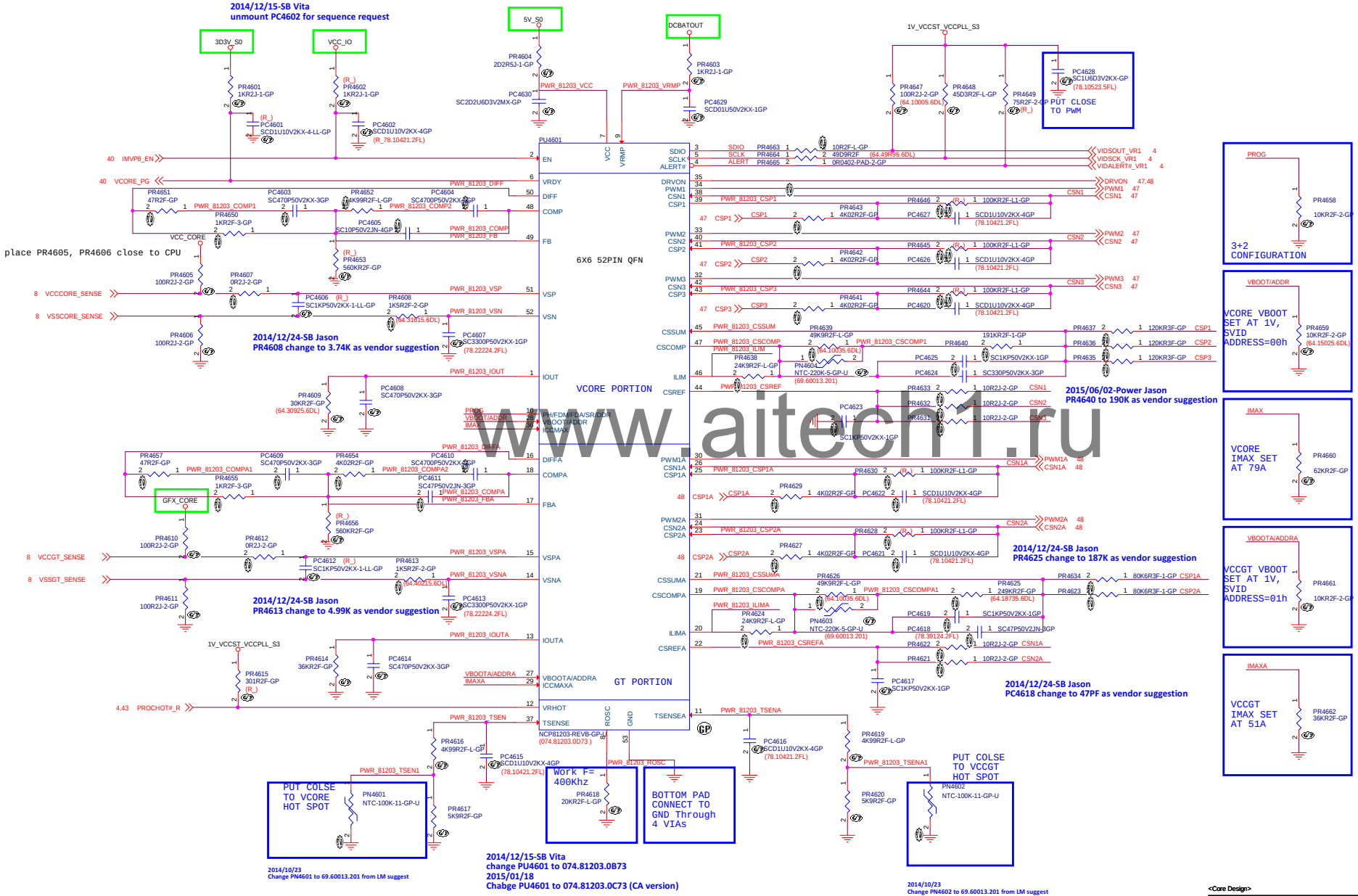
Hsichih, Taipei Hsien
Title: RT8243_5V/3D3V
Size: C | Document Number: Consumer AIO Woody | Rev: 5A
Date: Thursday, November 26, 2015 | Sheet 45 of 107

PWR_CORE/PWR_VCCGT

Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE 65Watt



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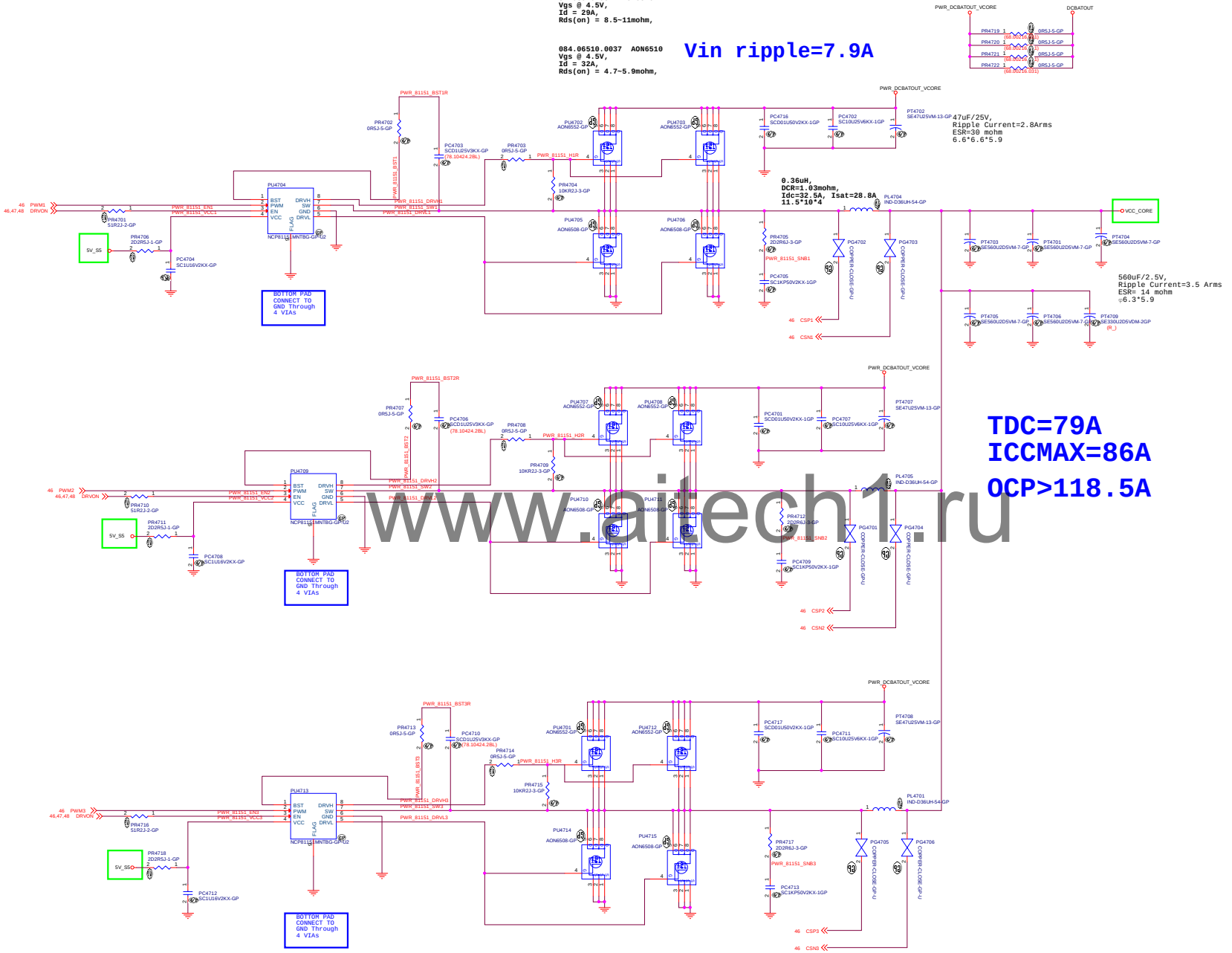
Title	VCORE & V_GT IC (NCP81203)	
Size C	Document Number: Consumer AIO Woody	Rev SA
Date: Thursday, November 26, 2015	Sheet 46 of 107	

PWR_CORE

84.06520.037 AON6520
Vgs @ 4.5V,
Id = 29A,
Rds(on) = 8.5~11mohm,

084.06510.0037 AON6510
Vgs @ 4.5V,
Id = 32A,
Rds(on) = 4.7~5.9mohm,

Vin ripple=7.9A



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Hsichih, Taipei Hsien

Title: VCORE OUTPUT (NCP81151)
Size: Custom | Document Number: Consumer AIO Woody | Rev: SA
Date: Thursday, November 26, 2015 | Sheet 47 of 107

PWR_VCCGT

84.06520.037 AON6520
Vgs @ 4.5V,
Id = 29A,
Rds(on) = 8.5~11mohm,

084.06510.0037 AON6510
Vgs @ 4.5V,
Id = 32A,
Rds(on) = 4.7~5.9mohm,

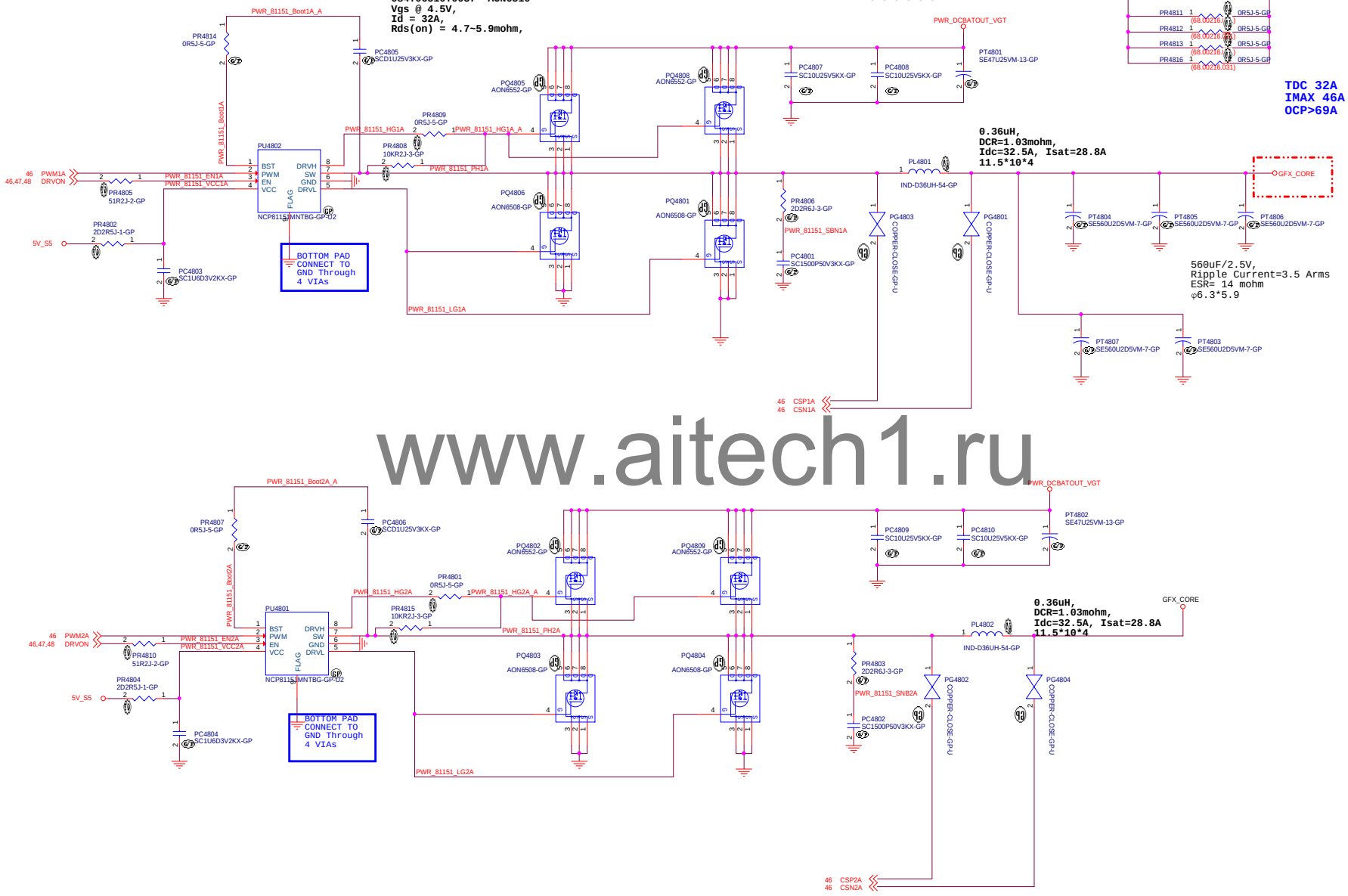
Input ripple current =6.39A
during Vout= 1.1V

47uF/25V,
Ripple Current=2.8Arms
ESR=30 mohm
6.6*6.6*5.9

TDC 32A
IMAX 46A
OCP>69A

0.36uH,
DCR=1.03mohm,
Idc=32.5A, Isat=28.8A
11.5*10*4

560uF/2.5V,
Ripple Current=3.5 Arms
ESR= 14 mohm
φ6.3*5.9



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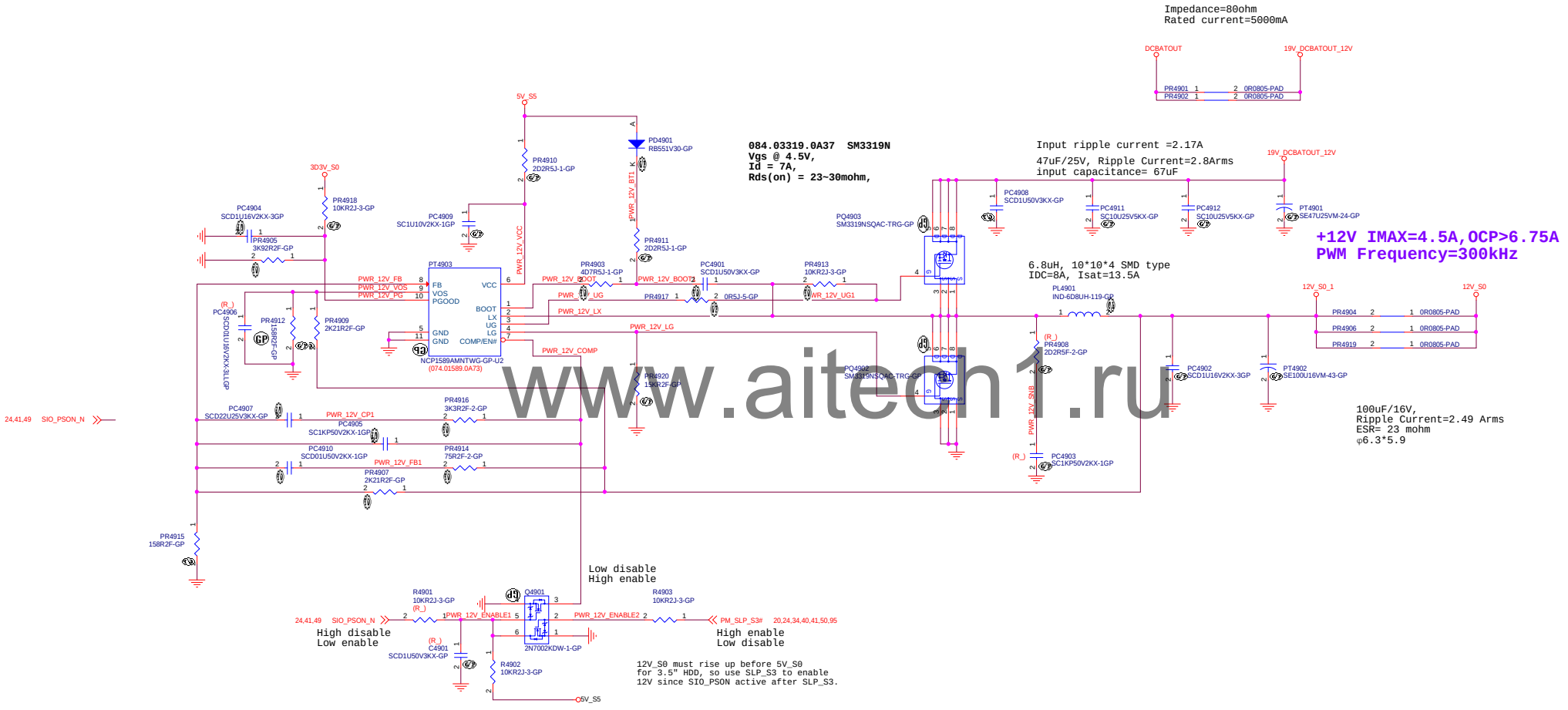
Title: V_GT OUTPUT(NCP81151)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 48 of 107

PWR_12V



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21F, 88, Sec.1,Hsin Tai Wu Rd
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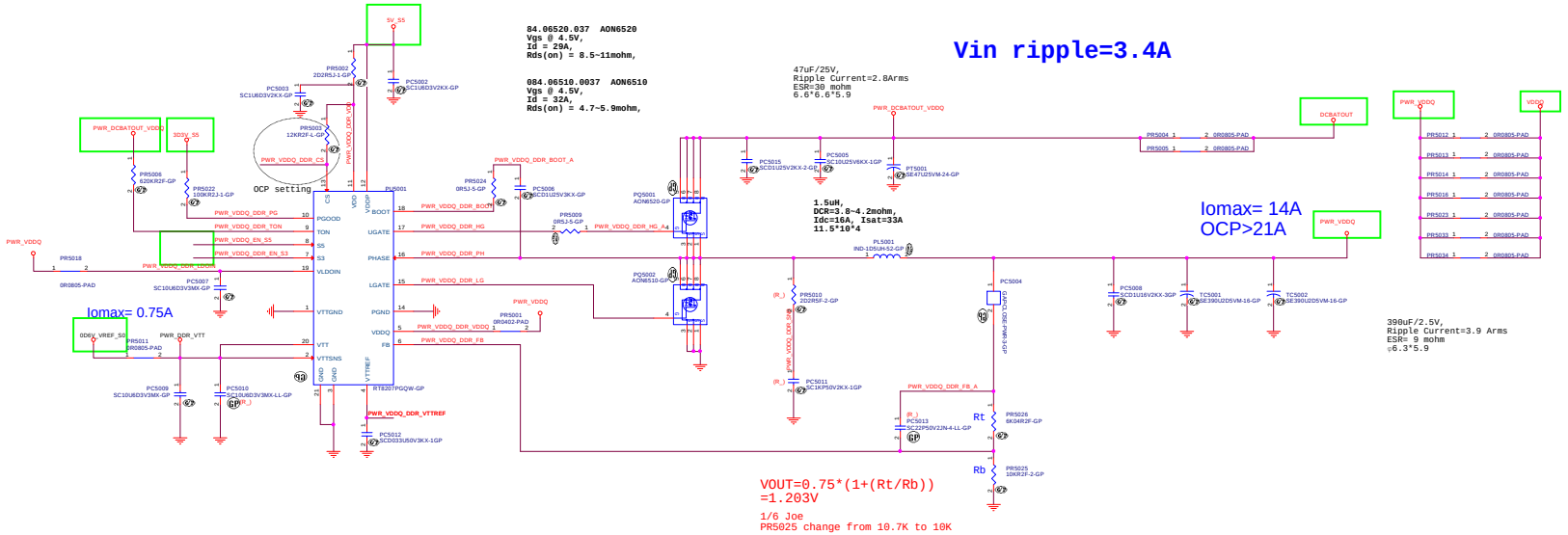
Title: DC to DC_12V (SY8246)

Size: C | Document Number: Consumer AIO Scotland | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 49 of 107

PWR_VDDQ



ENABLE SIGNAL

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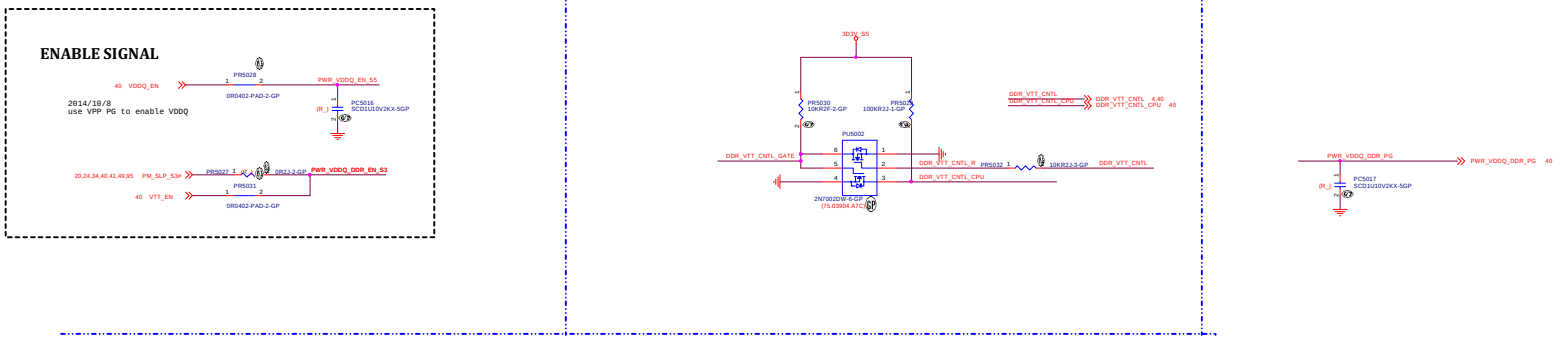
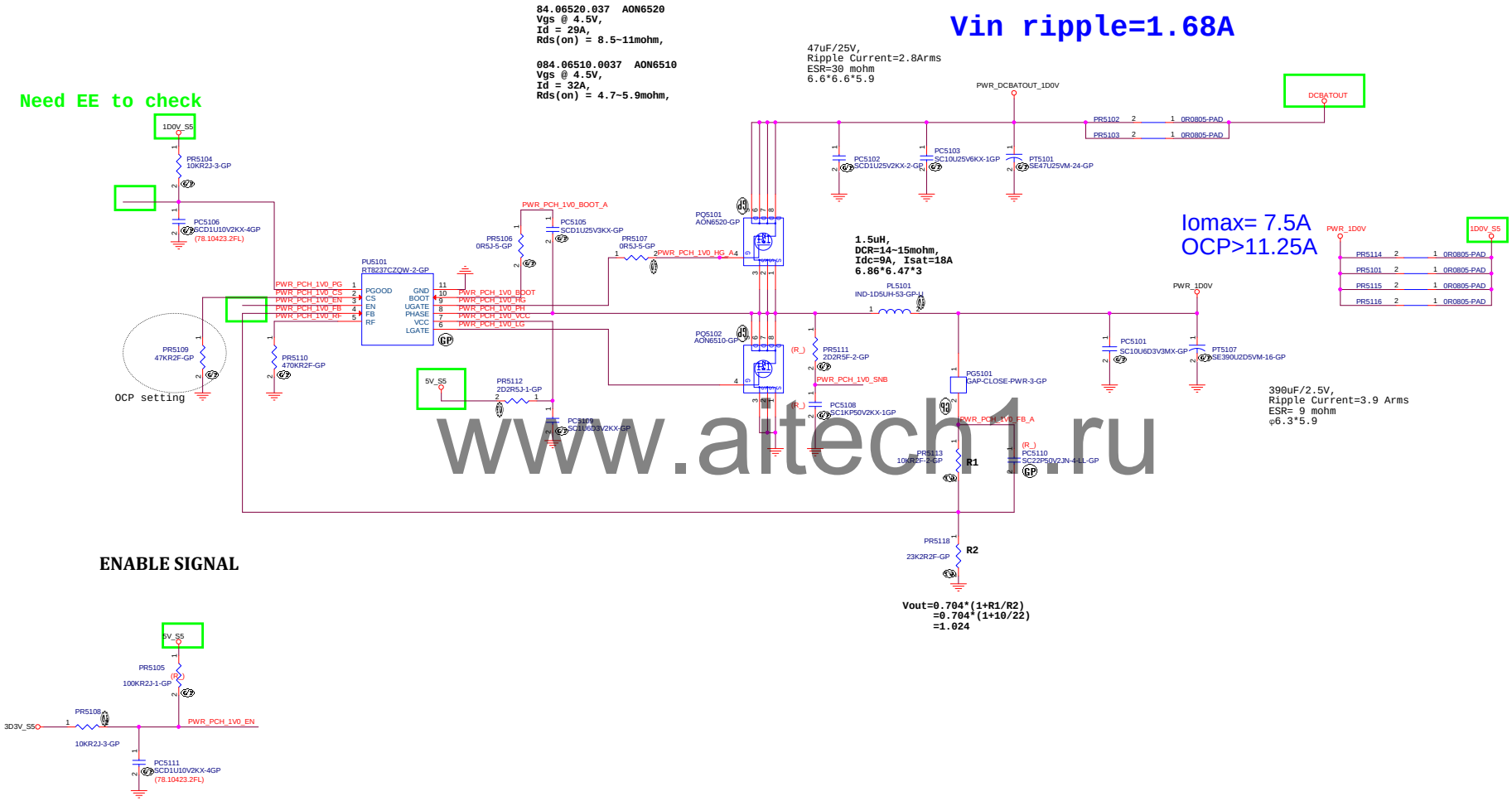


PWR_1D0V



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21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title	PCH_1P0V(RT8237C)	
Size: Custom	Document Number: Consumer AIO Scotland	Rev: SA
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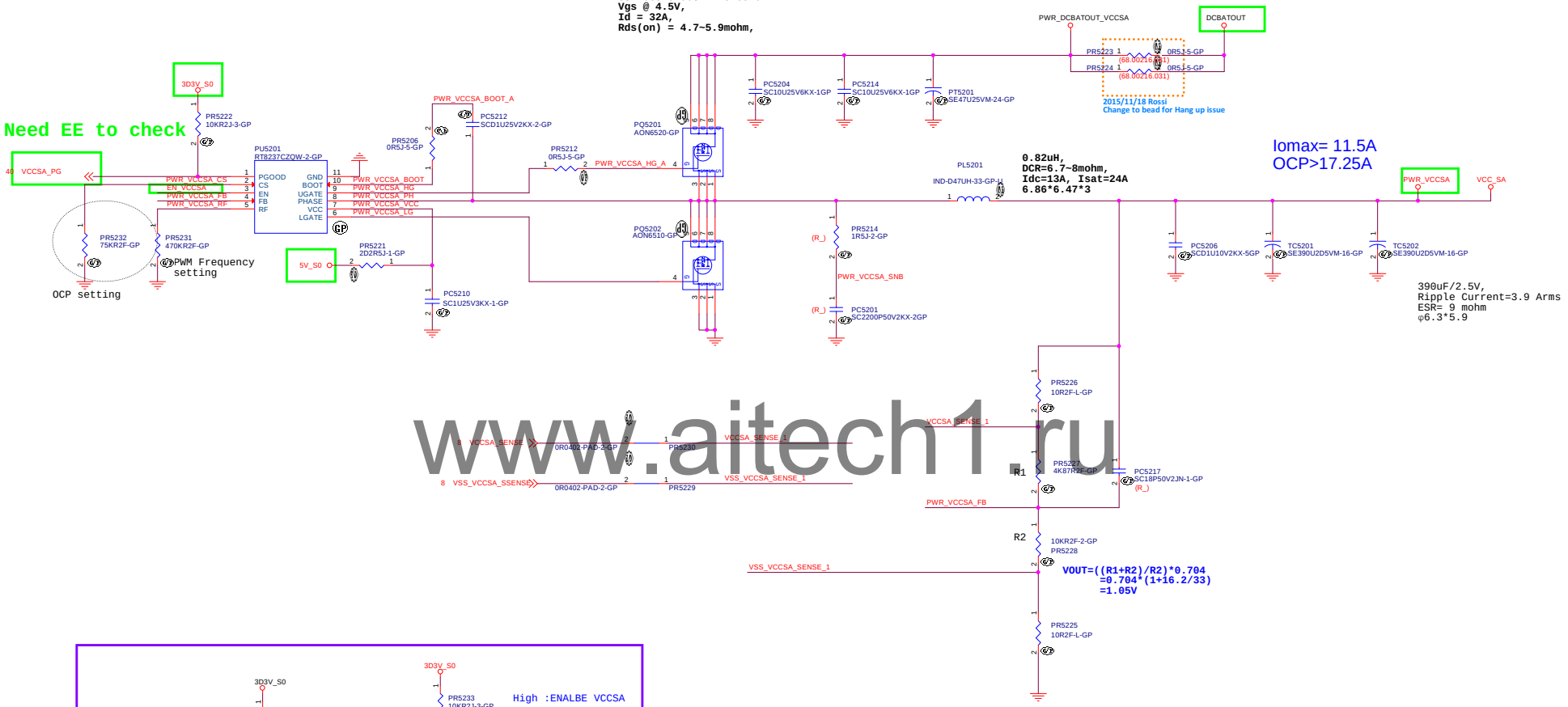
PWR_VCCSA

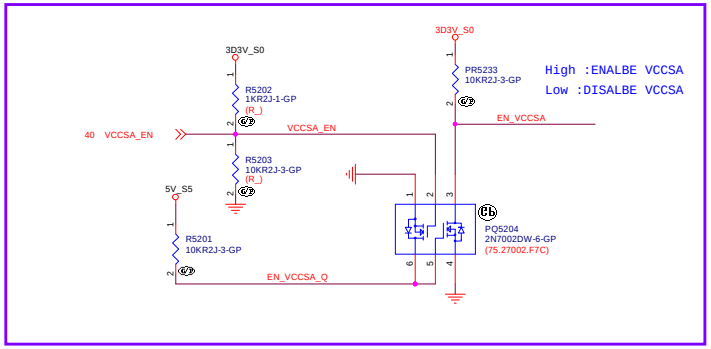
84.06520.037 AON6520
Vgs @ 4.5V,
Id = 29A,
Rds(on) = 8.5~11mohm,

084.06510.0037 AON6510
Vgs @ 4.5V,
Id = 32A,
Rds(on) = 4.7~5.9mohm,

Vin ripple=2.63A

Need EE to check





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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

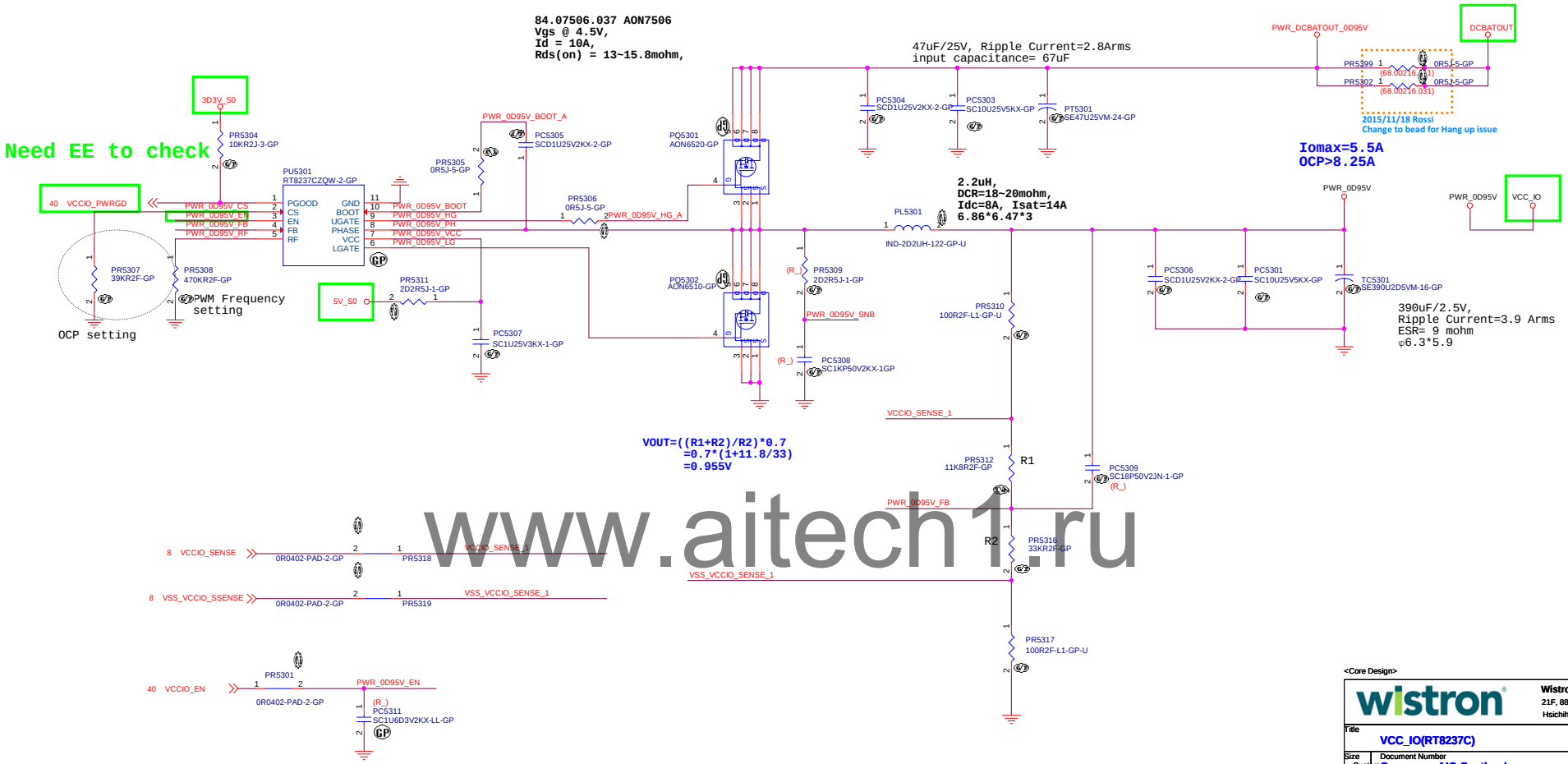
Title: VCC_SA(RT8237C)
Size: Custom
Document Number: Consumer AIO Scotland
Rev: SA
Date: Thursday, November 26, 2015
Sheet 52 of 107

PWR_VCCIO

84.07410.A37 SIS412DN
Vgs @ 4.5V,
Id = 7A,
Rds(on) = 24~29mohm,

84.07506.037 AON7506
Vgs @ 4.5V,
Id = 10A,
Rds(on) = 13~15.8mohm,

Vin ripple=1.2A



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21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: VCC_IO(RT8237C)

Size: Custom | Document Number: Consumer AIO Scotland | Rev: SA

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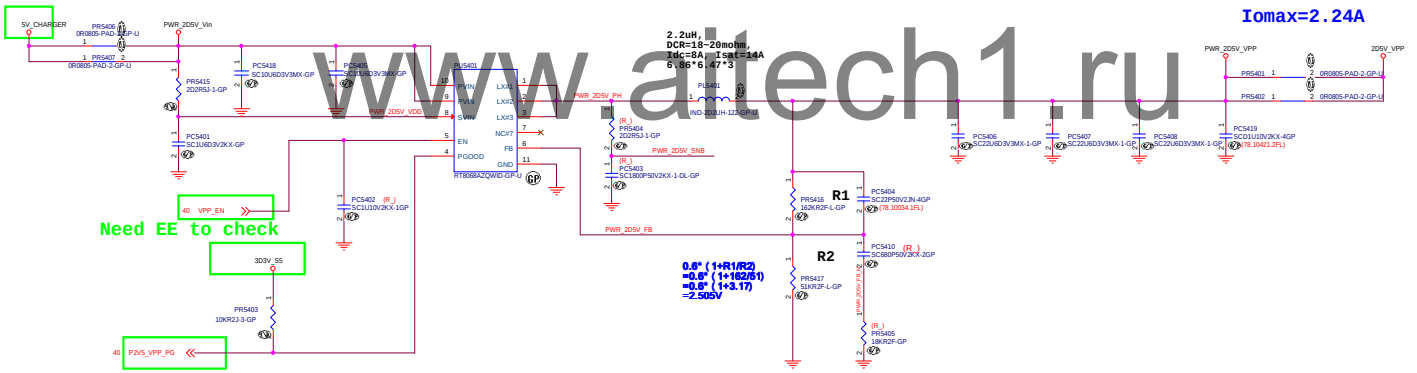
PWR_2D5V_VPP



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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LDO_1P5V_1P8V_2P5V

Size: Custom | Document Number: Consumer AIO Scotland | Rev: SA

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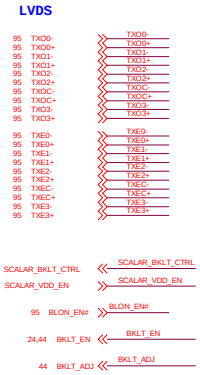
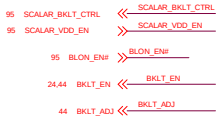
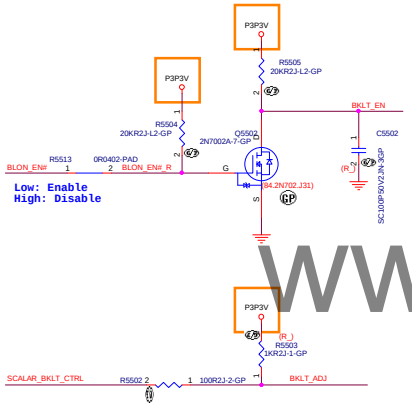
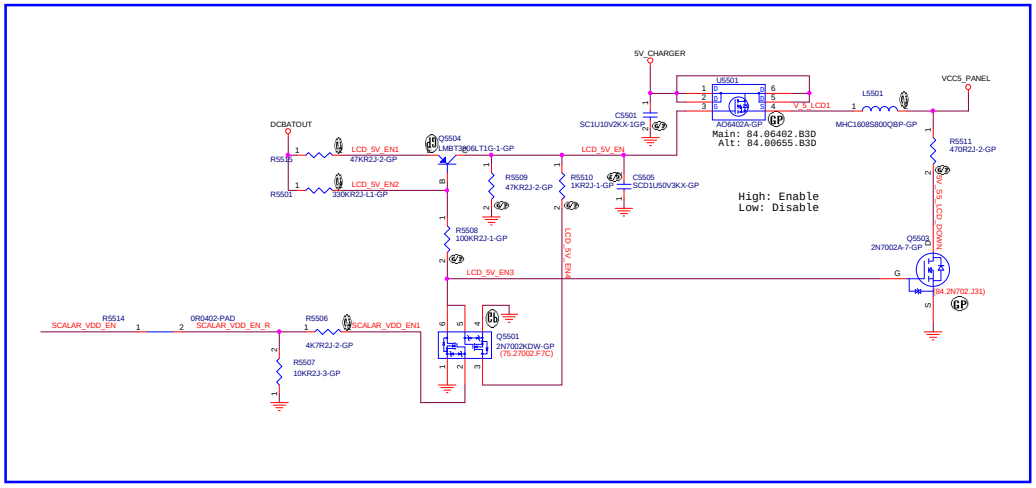
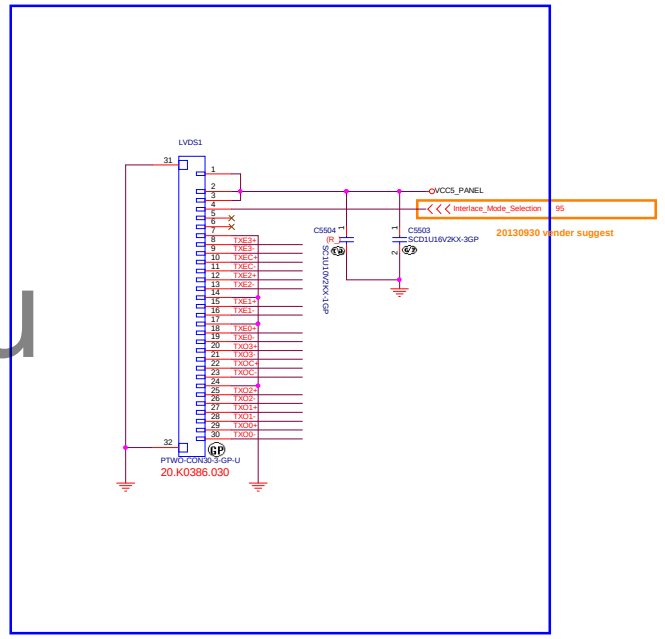
SSID = VIDEO











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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: LVDS Connector

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

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HDMI

56,95 HDMI1_D2+
56,95 HDMI1_D2-
56,95 HDMI1_D1+
56,95 HDMI1_D1-
56,95 HDMI1_D0+
56,95 HDMI1_D0-
56,95 HDMI1_CK+
56,95 HDMI1_CK-

24,56,95 DET_HDMI#

95 DDC_WP
56,95 HDMI1_SDA
56,95 HDMI1_SCL

95 HPD_SCA1

HDMI-IN Connector

HDIN1

HDMI1_D2+_C
HDMI1_D2-_C
HDMI1_D1+_C
HDMI1_D1-_C
HDMI1_D0+_C
HDMI1_D0-_C
HDMI1_CK+_C
HDMI1_CK-_C
DET_HDMI_C
HDMI_SCL_IN
HDMI_SDA_IN
HDMI_HPDET

24,56,95 DET_HDMI#
R5615 1KR2J-1-GP (M_)

HDMI_5V
HDMI_5V
C5604 SCD1U16V2ZY-2GP (R_)

SKT-HDMI19P-57-GP (M_)

HPD_SCA1
R5619 100R2J-2-GP (M_)

20130910 Ryan

EMI/ESD near Connector

D5603
HDMI1_D0+_C
HDMI1_D0-_C
HDMI1_CK+_C
HDMI1_CK-_C
SP3010-04UTG-GP (R_)

D5604
HDMI1_D1-_C
HDMI1_D1+_C
HDMI1_D2-_C
HDMI1_D2+_C
SP3010-04UTG-GP (R_)

EMI/ESD near Connector

HDMI_5V
3D3V_A
R5618 1KR2J-1-GP
20130930 vender suggest
R5616 10KR2J-3-GP (M_)
HPD_SCA1
DET_HDMI#
U5602 AZ23C6V2-1-GP

HDMI_SCL_IN
HDMI_SDA_IN
U5603 AZ23C6V2-1-GP

Reserved for HDMI re-Driver

V_1P5

08/11 Allen modify

U5605
INPUT
OUTPUT
ADJ/GND
AZ1117CR-ADJTRG1-GP-U (M_074.01117.0A38)

3D3V_A
C5608 SC10U10V5KX-2DLGP (M_78.10623.51L)
C5607 SCD1U16V2KX-3DLGP (M_78.10421.2FL)
V_1P5_HDMI

R2 R5627 180R3F-GP (M_)
1117_ADJ
R1 R5628 36R3F-GP (M_)

Vout = 1.25*(1+R1/R2)

3D3V_A
C5618 SCD1U16V2KX-3GP (M_)
C5617 SCD1U16V2KX-3GP (M_)

V_1P5_HDMI

Change to oohm for Debug

HDMI1_D0+_C R5621 R2J-2-GP HDMI1_DATA_IC_P0
HDMI1_D0-_C R5622 R2J-2-GP HDMI1_DATA_IC_N0
HDMI1_D1+_C R5623 R2J-2-GP HDMI1_DATA_IC_P1
HDMI1_D1-_C R5624 R2J-2-GP HDMI1_DATA_IC_N1
HDMI1_D2+_C R5625 R2J-2-GP HDMI1_DATA_IC_P2
HDMI1_D2-_C R5639 R2J-2-GP HDMI1_DATA_IC_N2
HDMI1_CK+_C R5640 R2J-2-GP HDMI1_DATA_IC_P3
HDMI1_CK-_C R5641 R2J-2-GP HDMI1_DATA_IC_N3

TPAD24 TP3404 1HDMI_SCL_IN_U5604
TPAD24 TP3405 1HDMI_SDA_IN_U5604

U5604
VDD33
VDDRX
VDDTX
VDDTA
I2C_CTL_EN
IN_D0P
IN_D0N
IN_D1P
IN_D1N
IN_D2P
IN_D2N
IN_CKP
IN_CKN
SCL_SRC
SDA_SRC
HPD_SRC
HPD_SNK
REXT
OUT_D0P
OUT_D0N
OUT_D1P
OUT_D1N
OUT_D2P
OUT_D2N
OUT_CKP
OUT_CKN
EQ/I2C_ADDR0
CFG/I2C_ADDR1
PRE
ISET
PD#
DCIN_EN/SCL_CTL
DDCBUF/SDA_CTL
SCL_SNK
SDA_SNK
GND
PS8407ATQFN40GTR2-A1-GP (M_)

HDMI1_LANE0_IC_DP
HDMI1_LANE0_IC_DN
HDMI1_LANE1_IC_DP
HDMI1_LANE1_IC_DN
HDMI1_LANE2_IC_DP
HDMI1_LANE2_IC_DN
HDMI1_LANE3_IC_DP
HDMI1_LANE3_IC_DN
EQ
CFG
PRE
ISET
U5604_PD_N
DCIN_EN
DDCBUF
HDMI1_SCL_U5604
HDMI1_SDA_U5604

TP3402 TPAD24
TP3403 TPAD24

HDMI_HDCP_READY
REXT
R5626 4K99R2F-L-GP (M_63.56234.1DL)

24,96 SCALAR_EN
R5643 0R2J-2-GP U5604_PD_N (M_)

mount if use

3D3V_A
R5630 4K7R2F-GP CFG (M_)
R5635 4K7R2F-GP DCIN_EN (M_)
R5629 4K7R2F-GP EQ (R_)
R5631 4K7R2F-GP ISET (R_)
R5632 4K7R2F-GP DDCBUF (M_)
R5636 4K7R2F-GP PRE (R_)
R5642 4K7R2F-GP HDMI_HDCP_READY (M_)

mount if use

V_1P5_HDMI
C5610 SCD01U50V2KX-1DLGP
C5609 SCD1U16V2KX-3DLGP (M_78.10324.2FL) (M_78.10421.2FL)
Near Pin 20, 31

V_1P5_HDMI
C5612 SCD01U50V2KX-1DLGP
C5611 SCD1U16V2KX-3DLGP (M_78.10324.2FL) (M_78.10421.2FL)
Near Pin 19

V_1P5_HDMI
C5614 SCD01U50V2KX-1DLGP
C5616 SCD1U16V2KX-3DLGP (M_78.10324.2FL) (M_78.10421.2FL)
Near Pin 19

V_1P5_HDMI
C5613 SCD01U50V2KX-1DLGP
C5615 SCD1U16V2KX-3DLGP (M_78.10324.2FL) (M_78.10421.2FL)
C5607 11/14 BOM cost
Near Pin 20, 31

5V_S0
R5617 0R0402-PAD (M_)

HDMI_CLK & DATA level shift
don't need from Scalar

DDC5V_HDMI_R
D5601 BAT54C-12-GP (M_75.00054.T7D)
DDC5V_HDMI

HDMI_5V
R5620 100KR2J-1-GP (M_)
D5602 BZX84-C6V8-GP (M_)

R5614 4K7R2J-2-GP
R5613 4K7R2J-2-GP
R5609 10KR2J-3-GP
(M_64.10015.60L)(M_64.10015.6DL)

HDMI_SCL_IN
HDMI_SDA_IN
R5610 47R2J-2-GP
R5611 47R2J-2-GP (M_)
DDC_WP_1

U5601
VCC
WC#
SCL
SDA
E0
E1
E2
VSS
M24C02-WMN6TP-1-GP (M_)

C5603 SCD1U16V2ZY-2GP (R_)

56,95 HDMI1_SDA
56,95 HDMI1_SCL

C5605 SC33P50V2JN-3GP (R_)
C5606 SC33P50V2JN-3GP (R_)

R5612 100R2J-2-GP (M_)
DDC_WP

C5601 DUMMY-C2
C5602 DUMMY-C2

TR5602
56,95 HDMI1_D0-
56,95 HDMI1_D0+
HDMI_LANE0_IC_DN
HDMI_LANE0_IC_DP
FILTER-4P-1-GP (M_66.R0036.04L)

TR5604
56,95 HDMI1_CK-
56,95 HDMI1_CK+
HDMI_LANE3_IC_DN
HDMI_LANE3_IC_DP
FILTER-4P-1-GP (M_66.R0036.04L)

TR5601
56,95 HDMI1_D2-
56,95 HDMI1_D2+
HDMI_LANE2_IC_DN
HDMI_LANE2_IC_DP
FILTER-4P-1-GP (M_66.R0036.04L)

TR5603
56,95 HDMI1_D1-
56,95 HDMI1_D1+
HDMI_LANE1_IC_DN
HDMI_LANE1_IC_DP
FILTER-4P-1-GP (M_66.R0036.04L)

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Title: HDMI IN
Size: C
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Pin#	Description	Type	Note
5	DVCC_33	Power	Digital power at 3.3V
9	VDD_DAC_33	Power	Analog power at 3.3V
19	VCCK_12	Power	Digital power at 1.2V
20	DVCC_33	Power	Digital power at 3.3V
24	AVCC_33	Power	Analog power at 3.3V
25	AVCC_12	Power	Analog power at 1.2V

7 DDI_VGA_AUX_CPU_P
7 DDI_VGA_AUX_CPU_N
7 DDI_VGA_DATA_CPU_P0
7 DDI_VGA_DATA_CPU_N0
7 DDI_VGA_DATA_CPU_P1
7 DDI_VGA_DATA_CPU_N1
16 CRT_HPD_PCH
24,44 SMBCLK2_SIO
24,44 SMBDAT2_SIO

DP to VGA converter: RTD2168

DDI EDP set DP INPUT by VBIOS

DDI_VGA_AUX_CPU_P (D_) C5816 1 — SCD1U16V2KX-3GP — DP_AUX_RTD2168_P
DDI_VGA_AUX_CPU_N (D_) C5817 1 — SCD1U16V2KX-3GP — DP_AUX_RTD2168_N
DDI_VGA_DATA_CPU_P0 (D_) C5812 1 — SCD1U16V2KX-3GP — DP_DATA_RTD2168_P0
DDI_VGA_DATA_CPU_N0 (D_) C5813 1 — SCD1U16V2KX-3GP — DP_DATA_RTD2168_N0
DDI_VGA_DATA_CPU_P1 (D_) C5814 1 — SCD1U16V2KX-3GP — DP_DATA_RTD2168_P1
DDI_VGA_DATA_CPU_N1 (D_) C5815 1 — SCD1U16V2KX-3GP — DP_DATA_RTD2168_N1

U5801

RTD2168_AVCC33 — 24 AVCC_33
RTD2168_AVCC12 — 25 AVCC_12
3D3V_RTD2168 — 5, 20 DVCC_33
19 VCCK_12
RTD2168_DAC33 — 9 VDD_DAC_33
RTD2168_LDO_EN — 21 LDO_EN
26 AUX_P
27 AUX_N
29 LANE0P
30 LANE0N
31 LANE1P
32 LANE1N
17 XI/CKIN
18 XO
RTD2168_RRX — 28 RRX
R5804 12KR2F-L-GP (D_)

1 HPD — DP_HPD_RTD2168
2 SMB_SCL — CIIC_SCL
3 SMB_SDA — CIIC_SDA
4 VGA_SCL — VGA_DDC_CLK
6 VGA_SDA — VGA_DDC_DATA
7 VSYNC — VGA_VSYNC
8 HSYNC — VGA_HSYNC
15 RED_P — VGA_RED_P
16 RED_N
12 GREEN_P — VGA_GREEN_P
13 GREEN_N
10 BLUE_P — VGA_BLUE_P
11 BLUE_N
22 POL1_SDA — POL1_SDA
23 POL2_SCL — POL2_SCL
14 GND_DAC
33 GND
RTD2168-CGT-GP (D_)

2013/10/23
Change L5312 & L5311 that follow Brian

3D3V_S0 — R5802 0R0603-PAD-2-GP-U — 3D3V_RTD2168
RTD2168 comsump max 0.6W (in spec) 3.3V @ <200mA
AC 60 ohm 1000mA — L5804 (D_) MHC1608S601LBP-GP — RTD2168_AVCC33
C5818 SC10U6D3V3MX-GP (D_) — C5825 SCD1U16V2KX-3GP (D_) — **pin24**
AC 60 ohm 1000mA — L5805 (D_) MHC1608S601LBP-GP — RTD2168_DAC33
(D_) C5821 SCD1U16V2KX-3GP — **pin5**
(D_) C5820 SCD1U16V2KX-3GP (D_) — **pin20**
C5819 (D_) SC10U6D3V3MX-GP — **pin24**
C5826 (D_) SCD1U16V2KX-3GP — **pin9**
C5827 (D_) SC10U6D3V3MX-GP — **pin9**
RTD2168_AVCC12
(D_) C5823 SCD1U16V2KX-3GP — **pin25**
(D_) C5822 SCD1U16V2KX-3GP — **pin19**
CRB suggest X5R
(D_) C5824 SC2D2U10V3KX-1GP — **pin19**

VGA cable
un-Plug: Low
Plug: High
DP_HPD_RTD2168
R5803 0R2J-2-GP
CRT_HPD_PCH
Q5801 2N7002H-GP (R_)
R5817 100KR2J-1-GP (D_)

eDP HPD active high

@. Check if need level shift for all signals
@. ESD solution follow Rosa Tigris

Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

3D3V_RTD2168 — R5812 4K7R2F-GP (R_) — POL1_SDA — R5811 4K7R2F-GP (D_)
3D3V_RTD2168 — R5814 4K7R2F-GP (D_) — POL2_SCL — R5813 4K7R2F-GP (R_)

RTD2168 Supports three operation mode for system design. Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode: PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

EEPROM MODE

In EEPROM mode,an additional EEPROM is needed.
EEPROM should configure with following conditions.

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

3D3V_RTD2168 — U5802 M24128-BWMN6TP-GP (D_)
POL2_SCL — SCL
POL1_SDA — SDA
VCC, WC#, E0, E1, E2, VSS

128Kbit, $0.1 too expensive
I2C address=0xA8

Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

3D3V_RTD2168 — R5805 4K7R2F-GP (D_) — RTD2168_LDO_EN — R5806 4K7R2F-GP (R_)

Select VCCK_V12 source from external 1.2V or embedded LDO

EP Mode

Pin2, Pin3 should be connected to EC for EP mode I2C protocol is used

2014/7/30 need check

RTD2168_SMBUS_ON
SMBCLK2_SIO — R5807 4K7R2F-GP (D_) — CIIC_SCL — R5809 4K7R2F-GP (R_)
SMBDAT2_SIO — R5818 0R2J-2-GP (R_) — SMB_DATA_2168 — R5819 0R2J-2-GP (R_) — R5808 4K7R2F-GP (D_) — CIIC_SDA — R5810 4K7R2F-GP (R_)
SMB_CLK_2168
Q5802 2N7002KW-GP (R_75.27002.F7C)
Q5803 2N7002KW-GP (R_75.27002.F7C)
3D3V_RTD2168

SMB_DATA_2168 — R5820 10KR2J-3-GP
SMB_CLK_2168 — R5821 10KR2J-3-GP
3D3V_A
RTD2168_SMBUS_ON — R5822 10KR2J-3-GP — 3D3V_S0
R5823 10KR2J-3-GP
RTD2168_SMBUS_ON default GPI, need pull down.

RTD2168 Slave Address: 0x64/0x65

VGA_RED_P — L5801 (D_) BLM18BB220SN-GP — CRT_R
VGA_GREEN_P — L5802 (D_) BLM18BB220SN-GP — CRT_G
VGA_BLUE_P — L5803 (D_) BLM18BB220SN-GP — CRT_B
2014/8/13 vendor suggest from 75ohm to 22ohm
R5827 75R2F-2-GP (D_)
R5828 75R2F-2-GP (D_)
R5829 75R2F-2-GP (D_)
C5802 C5807 C5808 C5809 C5810 C5811 C2CP50V2CN-GP (D_)
20140708 David vendor suggest from 10pF to 4.7pF
CRB suggest 75ohm
2014/8/13-SA Vita vendor suggest from 4.7pF to 2pF

5V_S0 — D5801 L1SS355T1G-GP (83.00355.D1F) — VGA_DDC_PU
2014/8/13-SA Vita DDC PU to 2.2K, follow vendor
R5825 2K2R2J-2-GP (D_)
R5826 2K2R2J-2-GP (D_)
VGA_DDC_DATA — R5801 (D_) 0R2J-2-GP — CRT_DDCDATA_CON
VGA_DDC_CLK — R5824 (D_) 0R2J-2-GP — CRT_DDCCLK_CON
20140708 David vendor suggest from 33 to 0ohm
C5903 (R_) C5906 (R_) C2CP50V2CN-3GP

VGA_HSYNC — R5815 (D_) 36R2J-GP — CRT_HSYNC_CON
VGA_VSYNC — R5816 (D_) 36R2J-GP — CRT_VSYNC_CON
C5805 (D_) C5804 (D_) SCD10P50V2JN-4GP

5V_S0 — F5801 POLYSW-1D5A8V-4-GP (D_) — 5V_VGA — L5806 MHC2012S221QBP-GP (D_) — 5V_S0_VGA
C5829 SCD1U16V2KX-3GP (D_)

2015/1/14-SB Vita
add L5607 for short test
change F2402 to 69.50007.D21 as DVI port

VGA1 D-SUB-15-130-GP
VCC_CRT, NC#4, NC#11
CRT_DDCDATA_CON — DDCDATA_ID1
CRT_DDCCLK_CON — DDCCLK_ID3
CRT_R, CRT_G, CRT_B
CRT_RED, CRT_GREEN, CRT_BLUE
CRT_VSYNC_CON — VSYNC
CRT_HSYNC_CON — HSYNC
GND

5V_S0_VGA — C5828 SCD1U16V2KX-3GP (R_)
VGA_DDC_PU — C5801 SCD1U16V2KX-3GP (R_)

ED5802 AZC099-04S-R7G-GP (D_075.00005.0B7C)
CRT_B — I/O1
GND
I/O2
CRT_G — I/O4
VDD
CRT_R — I/O3

ED5801 AZC099-04S-R7G-GP (D_075.00005.0B7C)
CRT_DDCCLK_CON — I/O1
GND
CRT_DDCDATA_CON — I/O2
CRT_VSYNC_CON — I/O4
VDD
CRT_HSYNC_CON — I/O3

2015/01/18-SB Corree
add ED6520 / ED2 as 075.00005.0B7C (EMI request)
2015/01/23-SB Vita
change ED6520 / ED2 F7 to (D_075.00005.0B7C)

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Title: DVI/CRT
Size: Custom
Document Number: Consumer AIO Woody
Rev: SA
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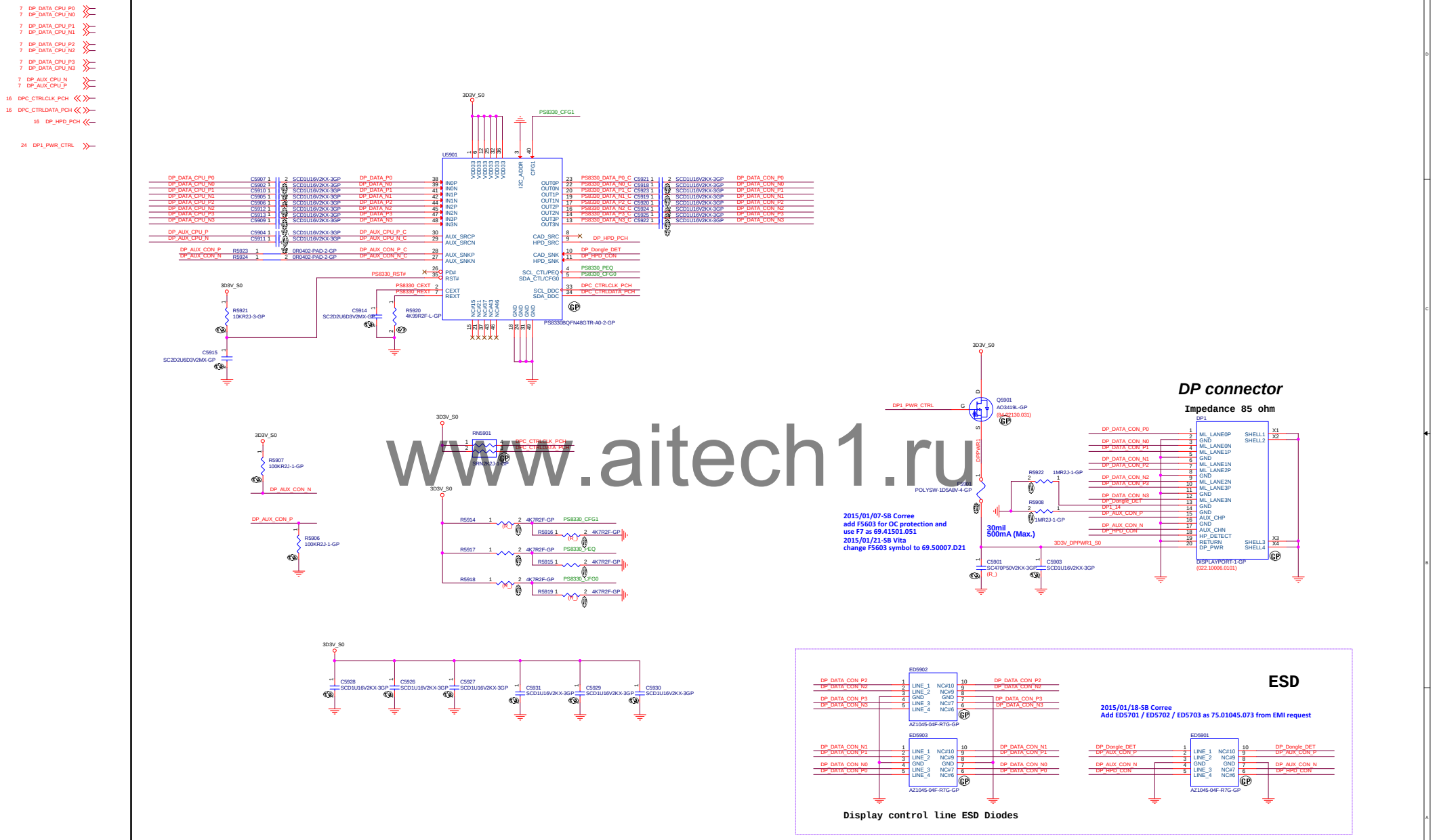

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Title: Display port

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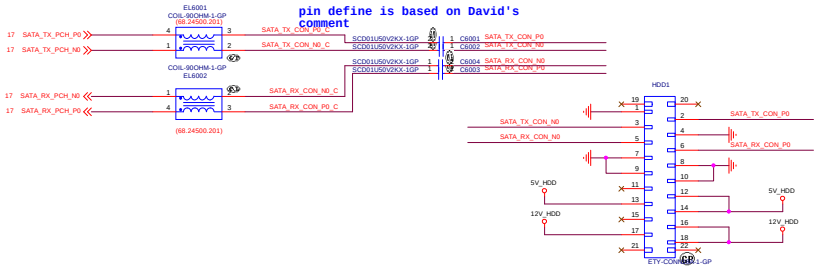
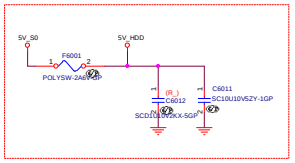
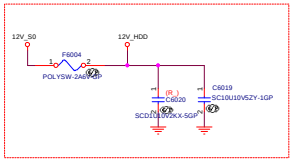
SATA Port 0

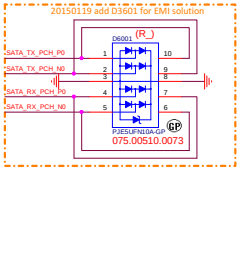
SATA HDD Connector

Michael 2012/01/03
pin define is based on David's comment



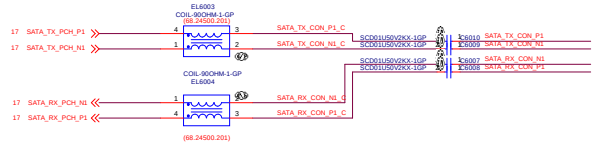


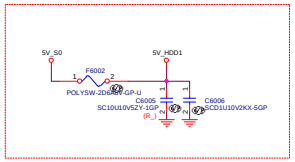


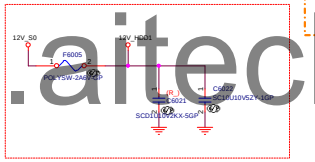


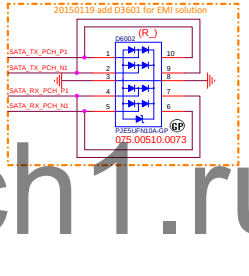
SATA Port 1

SATA HDD Connector



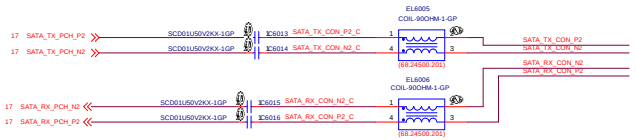


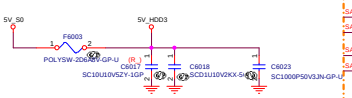


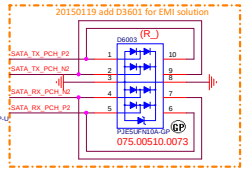


SATA Port 2

ODD Connector







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Title: HDD/ODD

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Title: Mini PCIE Card TV Tuner_(R)

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M.2 2230 / 1630 Key E Type

Mini PCIE (WLAN)

15 USB_PCH_PP7
15 USB_PCH_PN7

PCIEX1

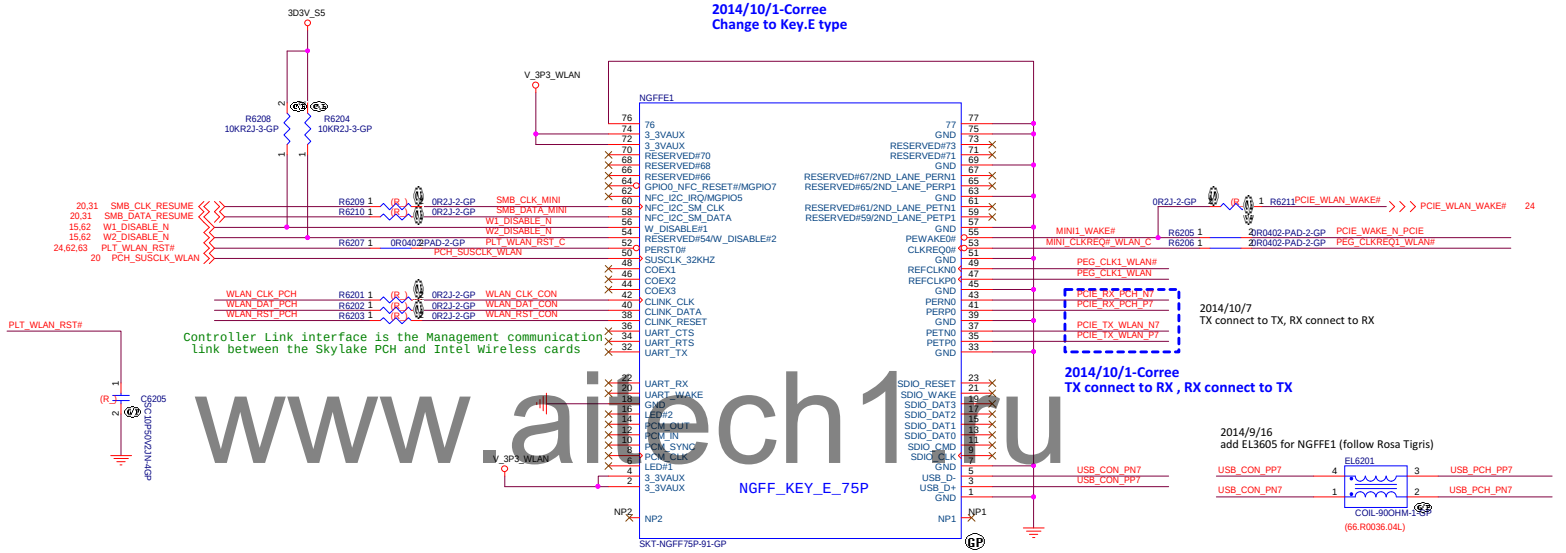
16 PCIE_RX_PCH_N7
16 PCIE_RX_PCH_P7
16 PCIE_TX_WLAN_N7
16 PCIE_TX_WLAN_P7

18 PEG_CLK1_WLAN
18 PEG_CLK1_WLAN#

OTHERS

20 PCIE_WAKE_N_PCIE
24,62,63 PLT_WLAN_RST#
18 PEG_CLKREQ1_WLAN#
15,62 W1_DISABLE_N
15,62 W2_DISABLE_N
17 WLAN_RST_PCH
17 WLAN_DAT_PCH
17 WLAN_CLK_PCH

20 SLP_WLAN_N — SLP_WLAN_N
24,97 LAN_EN_PWR_SIO — LAN_EN_PWR_SIO



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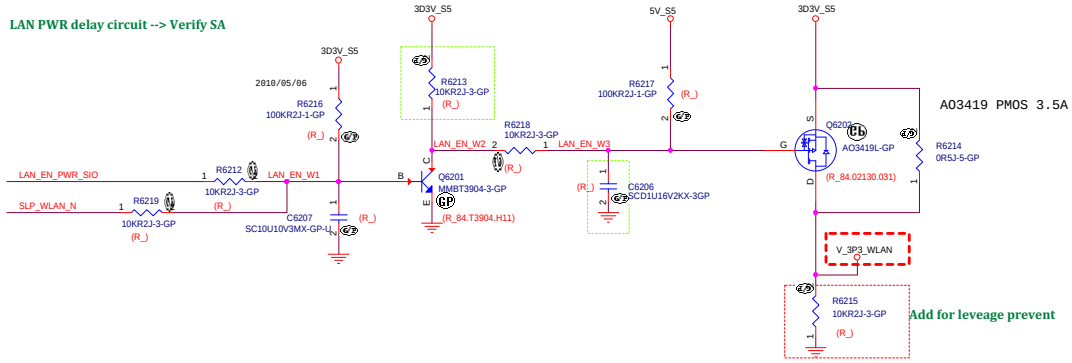
LAN Power

LAN PWR delay circuit --> Verify SA



WLAN (M2 key E)

HS5 STF256R109H124-GP

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Hsichih, Taipei Hsien

Title: WLAN and BT--NGFF

Size	Document Number	Rev
C	Consumer AIO Woody	SA

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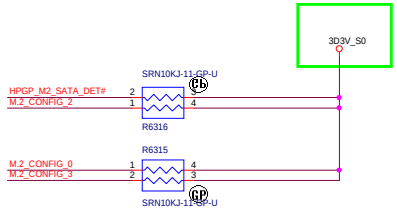
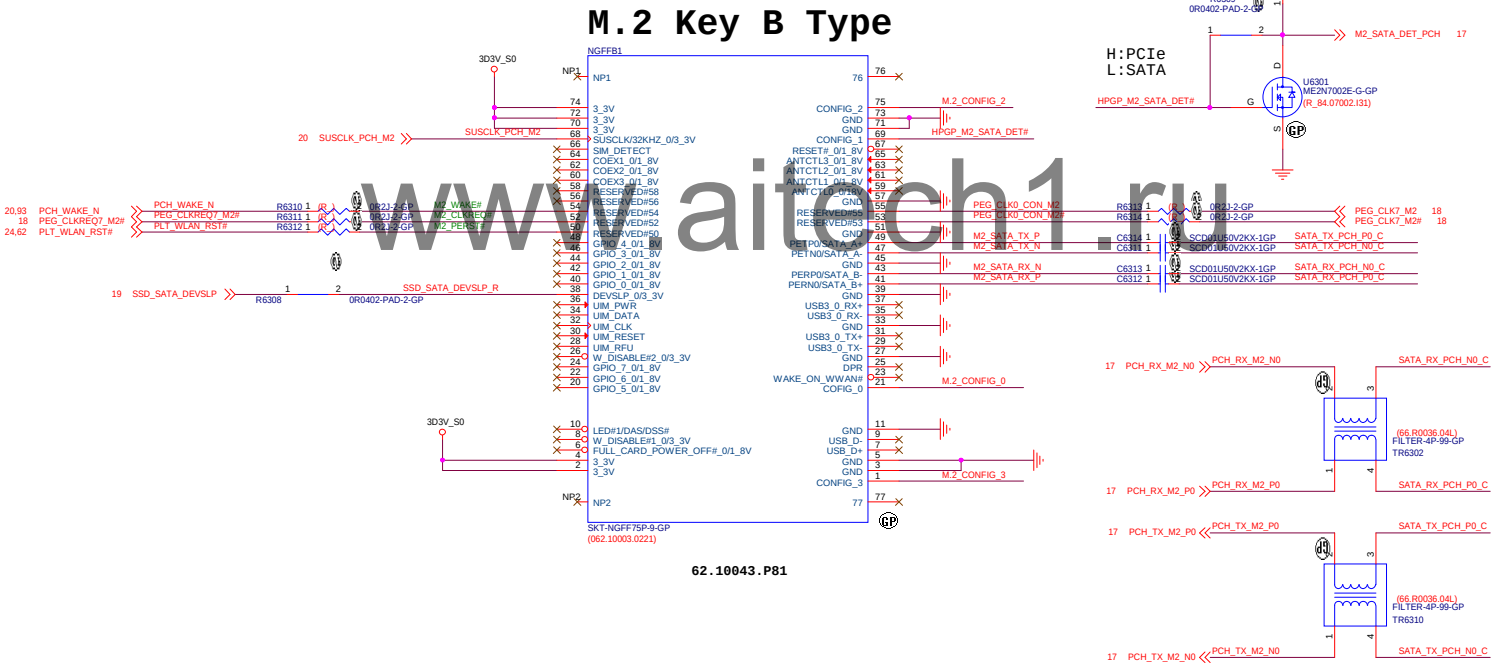
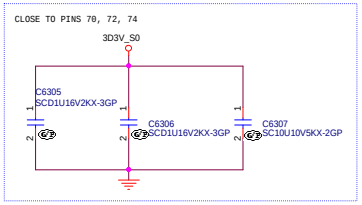
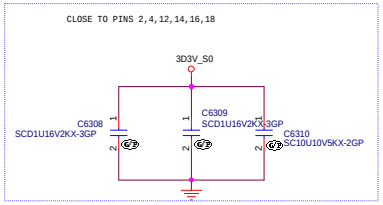
Table 46. Socket 2 Module Configuration Table

Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN – PCIe	0









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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

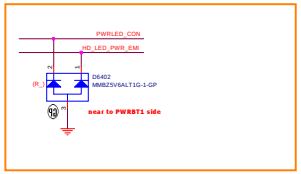
Title: SSD-NGFF

Size: C | Document Number: Consumer AIO Woody | Rev: SA

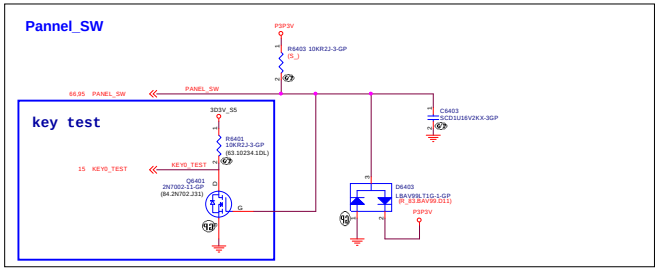
Date: Thursday, November 26, 2015 | Sheet 63 of 107

PWR BTN

20141203 Add D1 prevent ESD when Fab assembly



Pannel_SW



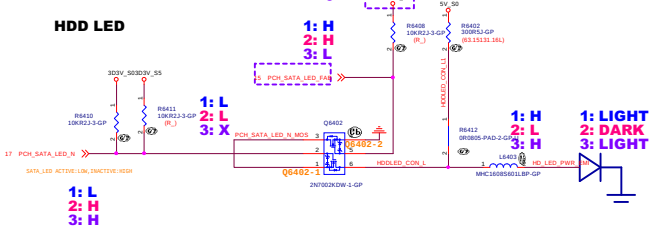
20141204 Modify HDDLED control logic

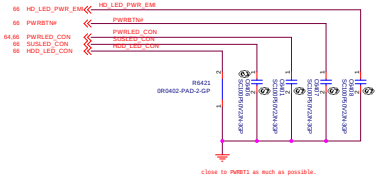
STATE	PCH_SATA_LED_N	PCH_SATA_LED_FAB	PCH_SATA_LED_N_MOS	Q6402-1	Q6402-2	HDDLED_CON	LED
1	L	H	L	OFF	ON	H	LIGHT
2	H	H	L	ON	ON	L	DARK
3	H	L	X	OFF	OFF	H	LIGHT

Note: 3. for FAB HDDLED test,
PCH_SATA_LED_FAB default is GPO High

20150115 Ryan

HDD LED

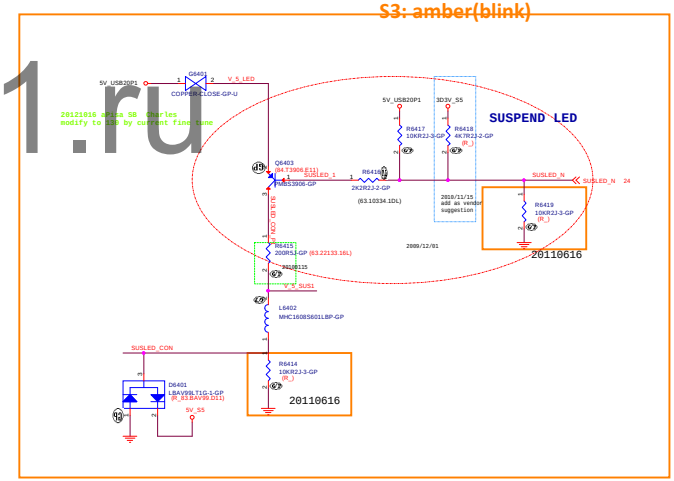




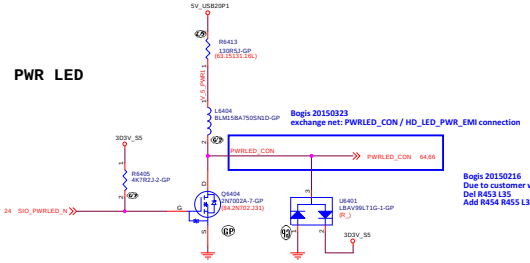
20150109 modify PWRLED behavior

S0: white(keep light)

~~S3: amber(blink)~~



PWR LED



Bogis 20150216
Due to customer want to add PC health function, so modify PWRLED control from 5V_S0 to ECIO GPIO pin.62
Del R453 L35
Add R454 R455 L36 Q54 U23

System LED Definition

S0/S1(Blue), S3(amber), S4(off), S5(off)

	S0	S3	S4/S5
SUSLED_N	LOW	HIGH	HIGH
SIO_PWRLED_N	LOW	HIGH	HIGH

PC Health LED Definition

POWER/ SUSLED Warning LED

	Normal		Warning		OFF
	S0	S3	S0	S3	S4/S5
SUSLED_N	HIGH	H & L PWM (Breathing)	H & L (Blinking)	H & L (Blinking)	HIGH
SIO_PWRLED_N	LOW	HIGH	LOW	LOW	HIGH

S0/Good (Blue)
S0/Warning (Blink Red)
S3/Good (Blink Blue)
S3/Warning (Blink Red)
S4/S5 (off)

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wistron Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien
Title: PWR BT/Side Key/LED
Size: D
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
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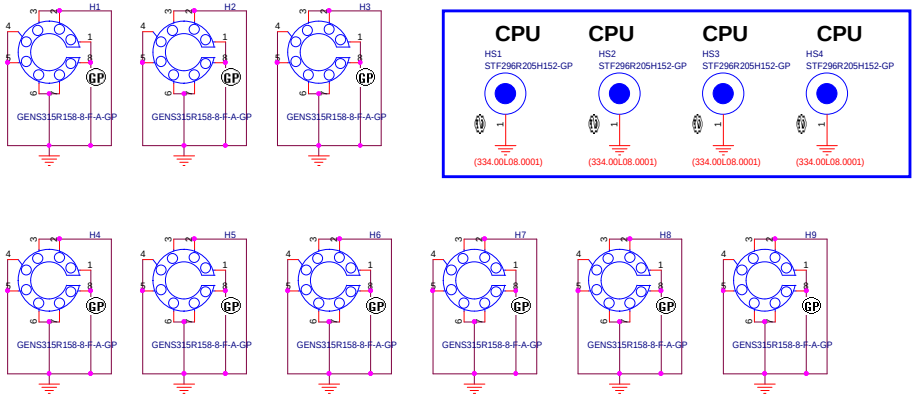
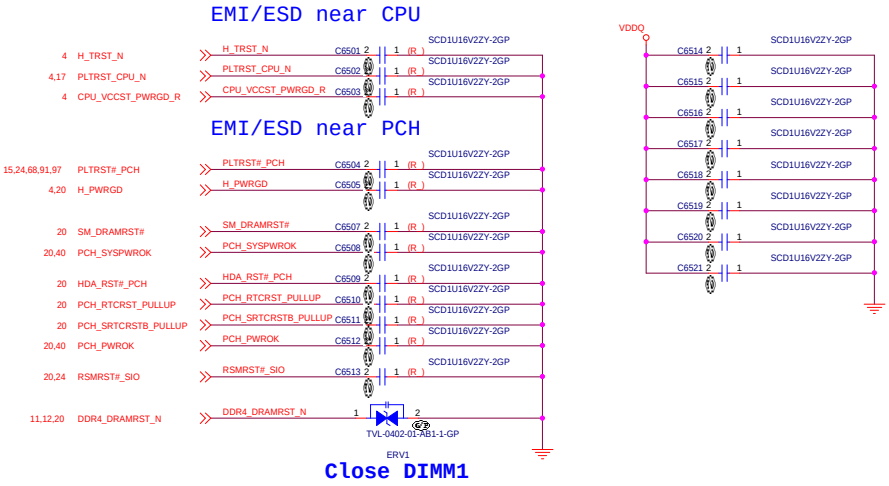
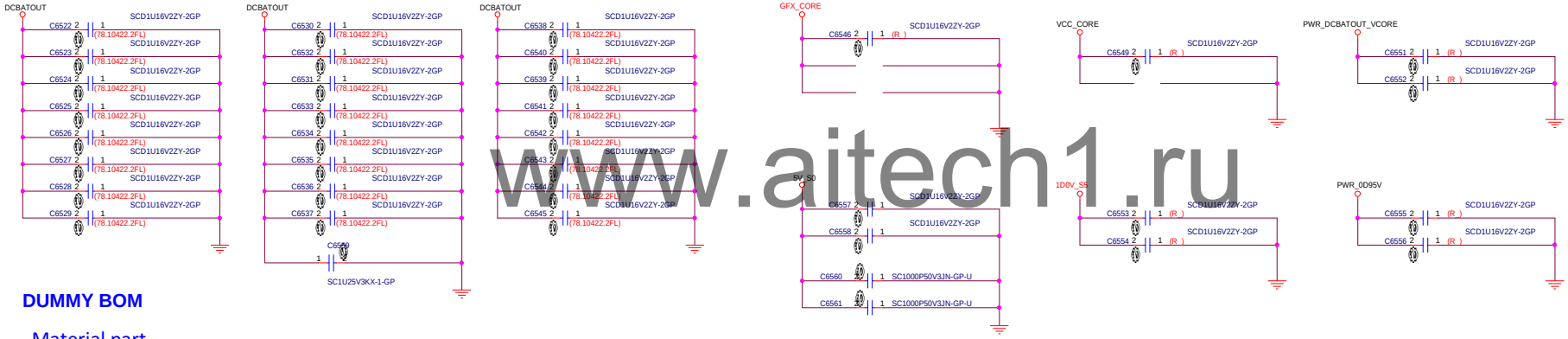
Stand off&Hole



EMI CAP



Close DIMM1



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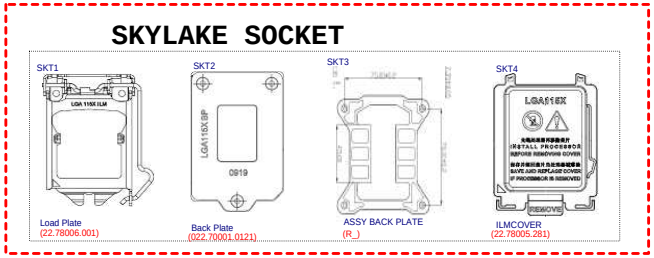
DUMMY BOM

Material part



GSKT1
GASKET
(R_334.03508.0001)

GASKET FOR WIESON HDMI

GSKT2
GASKET
(R_334.0350F.0001)

GASKET FOR TCONN HDMI

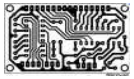
Del PCHHS1 by Thermal--Ryan 0225

Battery Symbol

BAT3
BATTERY CR2032
(R_23.20068.001)

Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001

PCB Symbol



PCB1
PCB
(R_)

HeatSink Symbol

PCHHS1
HEATSINK
(60.3ET05.001)

Vendor
P/N:
60.3MN01.011(second source)
60.3MN01.001

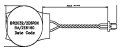
LABEL

LBL1
LABEL
(40.3BZ24.011)

LBL6
LABEL
(R_45.3J904.011)

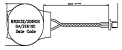
LBL5
LABEL
(R_40.3BZ24.001)

MB serial NO# and MAC address
40.3BZ24.011 -> 30 x 15mm
40.3KP03.011 -> 35 x 15mm
45.41107.021 -> 70 x 8mm
CARD
45.ACA01.0C1 -> 32 x 7mm
MIC CARD
45.41109.001 -> 20 x 5mm



BAT1
BATTERY CR2032_30MM
(23.21221.024)
Wire Length:30mm

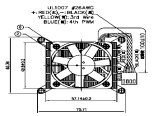
Vendor
P/N:
23.21221.024
23.21212.031



BAT2
BATTERY BR2032_60MM
(R_23.24220.612)
Wire Length:60mm
耐高溫>85C

Vendor
P/N:
23.21208.061
23.24220.612

HeatSink+FAN Symbol



HSFAN1
(R_60.3KN01.001)

Vendor
P/N:

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wistron
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21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Stand off&EMI Cap&DUMMY BOM

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USB3 Charger

USB30_RX_CON_N1 → USB30_RX_CON_N1 34, USB30_RX_CON_P1 → USB30_RX_CON_P1 34
USB30_TX_CON_N1 → USB30_TX_CON_N1 34, USB30_TX_CON_P1 → USB30_TX_CON_P1 34
USB_CON_PN1 → USB_CON_PN1 34, USB_CON_PP1 → USB_CON_PP1 34

Card Reader

16 USB_PCH_PP9
16 USB_PCH_PN9

Audio

30 HP_OUT_R_CON
30 HP_OUT_L_CON
28,30,95 JD_LOT
30 MIC_IN_L_JK
30 MIC_IN_R_JK
27 MIC_IN_JD

BTNBD

15 OBR
64 PWRBTN#
64 PWRLED_CON
64 SUSLED_CON
64 HDD_LED_CON

HDD/LAN LED

24 LAN_LED3_CTRL
31,32,97 LAN_LINKACTIVITY_LAN_N

ON/OFF

64,95 PANEL_SW

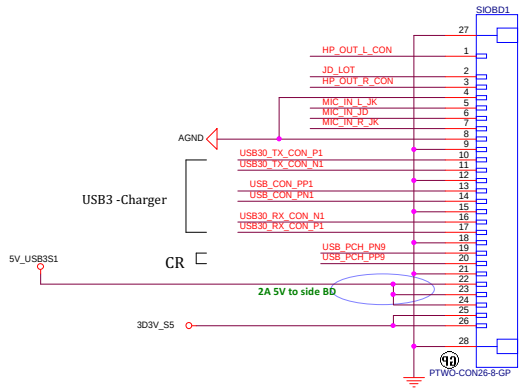
BRIGHTNESS

24 BRIGHTNESS_N

64 HD_LED_PWR_EMI → HD_LED_PWR_EMI

Side IO BD

2012/09/03
FFC1 (CR, USB3, Audio) 26pin

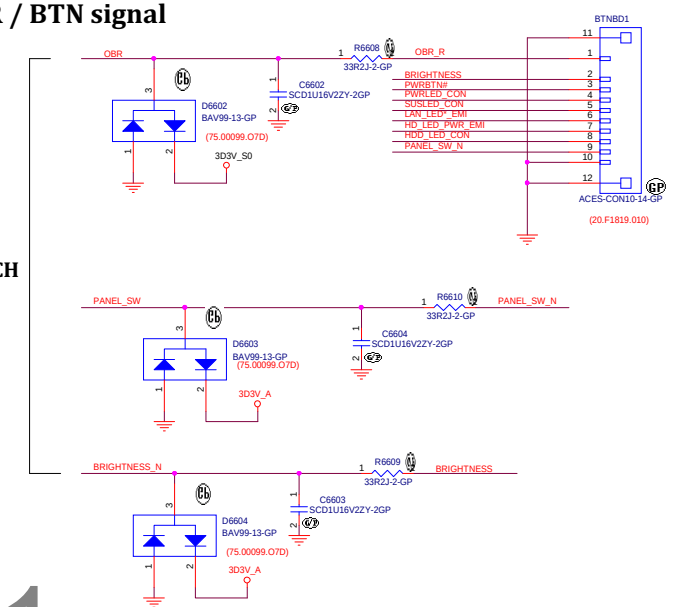


2013/04/21
Rossi delete FFC2

Button BD

OBR / BTN signal

To PCH



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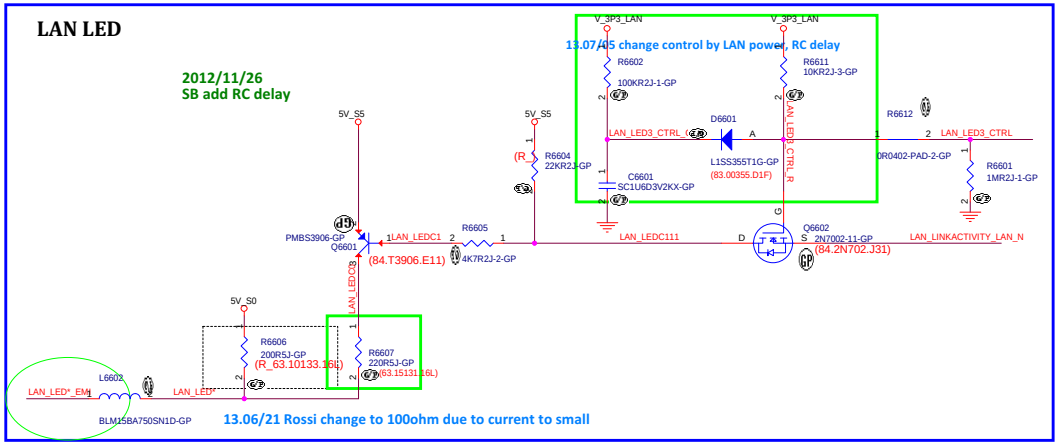
LAN LED

2012/11/26
SB add RC delay

13.07/05 change control by LAN power RC delay



13.06/21 Rossi change to 100ohm due to current to small

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Hsichih, Taipei Hsien

Title: IO Board
Size: C
Document Number: Consumer AIO Woody
Rev: SA
Date: Thursday, November 26, 2015
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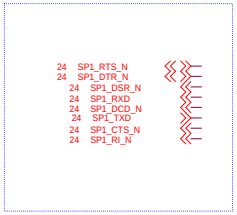
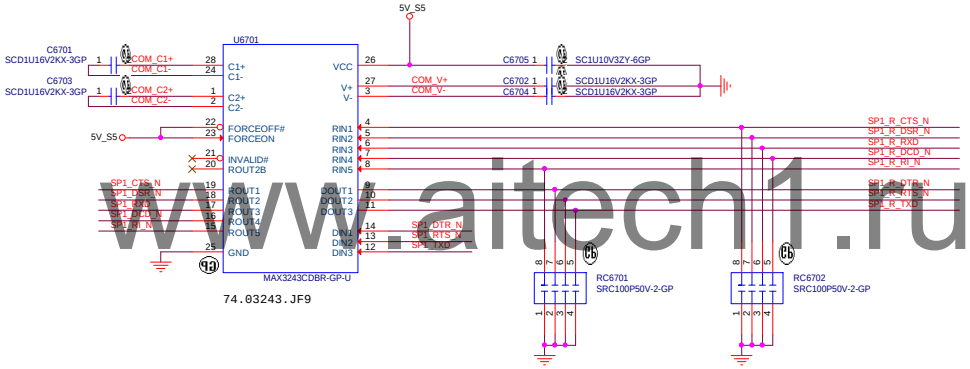
COM Port



2014/9/30-SA Vita
change COM2 power to +5V_AUX2

SERIAL PORT



74.03243.JF9

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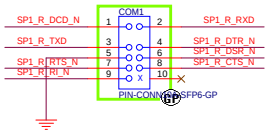
COM port header

13.07/05 Change comport to 2.0 pitch type



2014/8/7
change COM2 to 21.62884.205

2014/12/18-SB Vita
Change COM2 front header naming to COM1

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Hsichih, Taipei Hsien

Title: COM

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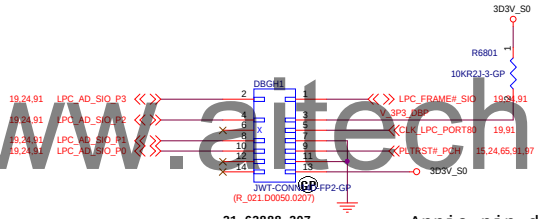
80 port Layout close to SIO



21.62888.207

Annie pin define

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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Debug

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Hsichih, Taipei Hsien

Title: LPT_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

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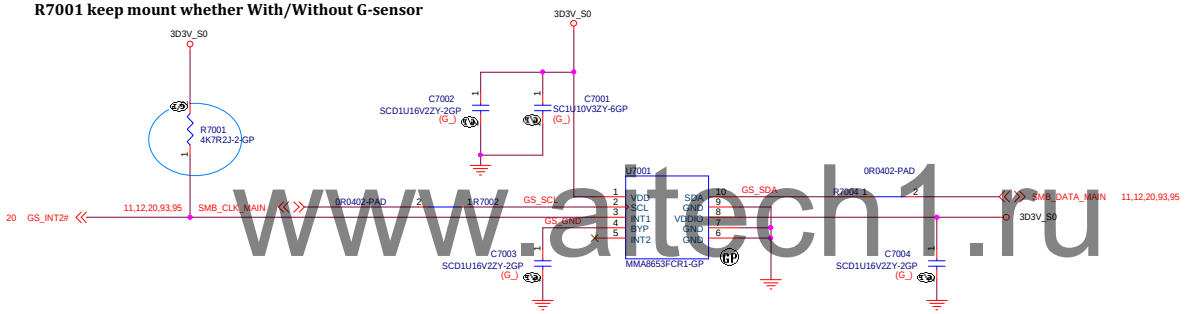
R7001 keep mount whether With/Without G-sensor



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21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: G sensor

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 70 of 107

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Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 72 of 107

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Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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Hsichih, Taipei Hsien

Title: Thunderbolt_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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Hsichih, Taipei Hsien

Title: GPU_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

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Hsichih, Taipei Hsien

Title: GPU_(R)

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(R)

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<Core Design>

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21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: 5A

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(R)

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<Core Design>

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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: SA

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(R)
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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 1&2_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: SA

Date: Thursday, November 26, 2015 | Sheet 81 of 107

(R)

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<Core Design>

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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 3&4_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: SA

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(R)
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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 5&6_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: 5A

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(R)

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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU VRAM 7&8_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: SA

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(R)
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<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU CORE_(R)

Size: D | Document Number: Consumer AIO Woody | Rev: SA

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(R)

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wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU discrete power_(R)

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

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wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Switch

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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Wistron Incorporated
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Hsichih, Taipei Hsien

Title: GPU Switch

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Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: GPU Others

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: NFC

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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19,24,68 LPC_FRAME#_SIO — LPC_FRAME#_SIO

19,68 CLK_LPC_PORT80 — CLK_LPC_PORT80

15,24,65,68,97 PLTRST#_PCH — PLTRST#_PCH

19,24,68 LPC_AD_SIO_P3 — LPC_AD_SIO_P3

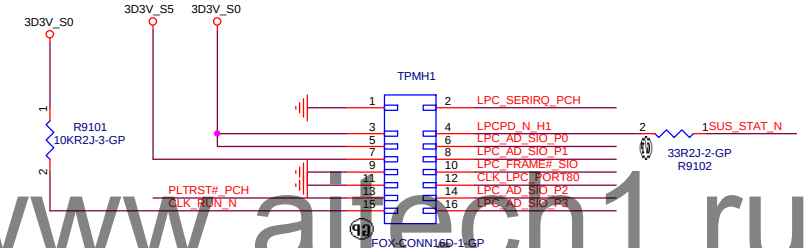
19,24,68 LPC_AD_SIO_P2 — LPC_AD_SIO_P2

19,24,68 LPC_AD_SIO_P1 — LPC_AD_SIO_P1

19,24,68 LPC_AD_SIO_P0 — LPC_AD_SIO_P0

19 SUS_STAT_N

19,24 LPC_SERIRQ_PCH



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Hsichih, Taipei Hsien

Title: TPM

Size: Custom | Document Number: Consumer AIO Woody | Rev: SA

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Hsichih, Taipei Hsien

Title: PS2_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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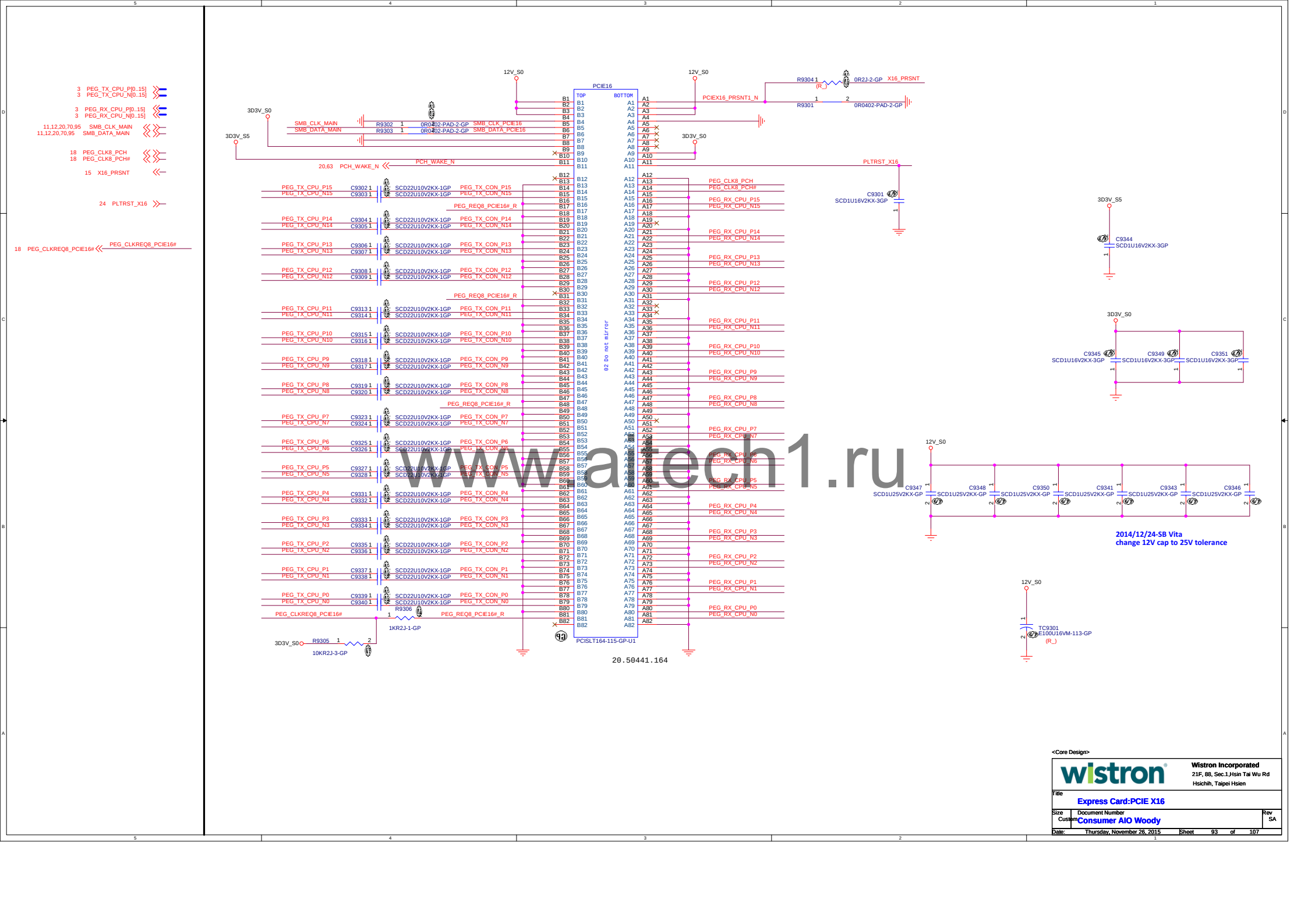

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Title: Smart Card_(R)

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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SSID = Scalar

Audio Out

LVDS-OUT

DMMI-IN

COMRTOL

BEAD 要30ohm@100MHz(1A)

如果有使用OD，建議在這邊放10uF(MLCC)

Main EEPROM

Shielding

Need Check

Michael 2012/2/6

EEPROM for OSD

72.24C16.Y01, ATMEL
72.02416.B01, ST

LCD ON/OFF

Pin 118
PW ON Latch功能選項
Internal MCU :Pull High
External MCU :Pull Low

B-EVEN

A-ODD

Remove

SB add

20150115 Ryan

To AMP

HDMI side:
HDMI0 => RX2 pair
HDMI1 => RX1 pair
HDMI2 => RX0 pair
HDMICK => RC pair

Monitor mode

Monitor	DET_HDMI#	SCALAR_EN	Panel EN/PWM/CTRL
	0	1	Active

DET_HDMI# : Connect to SIO and Scaler

To SIO: make scaler workable to switch EN 1(From SIO)

To Scaler: let scaler know HDMI-5V, and make related signal active, Panel and AMP

cDP-IN

Panel On Off CTRL

PC_MONITOR_SW

According to the IR decode or side key value to switch the satus of monitor mode and PC mode

Prevent leakage

Firmware update by SMBUS

Michael 2011/12/01
PC Mode + DVI使用在SO + 4個都用 3D3V_S0

SMBUS_ISP H : Simutaneous Mode
SMBUS_ISP L : Isolate Mode

Michael 2012/3/8 -A
R3205 is add for tune equal length

20150127 add 2N7002 logic for leakage

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Title: Scalar-RTD2486VRD
Size: A3
Document Number: Consumer AIO Woody
Rev: 0A
Date: Thursday, November 29, 2012
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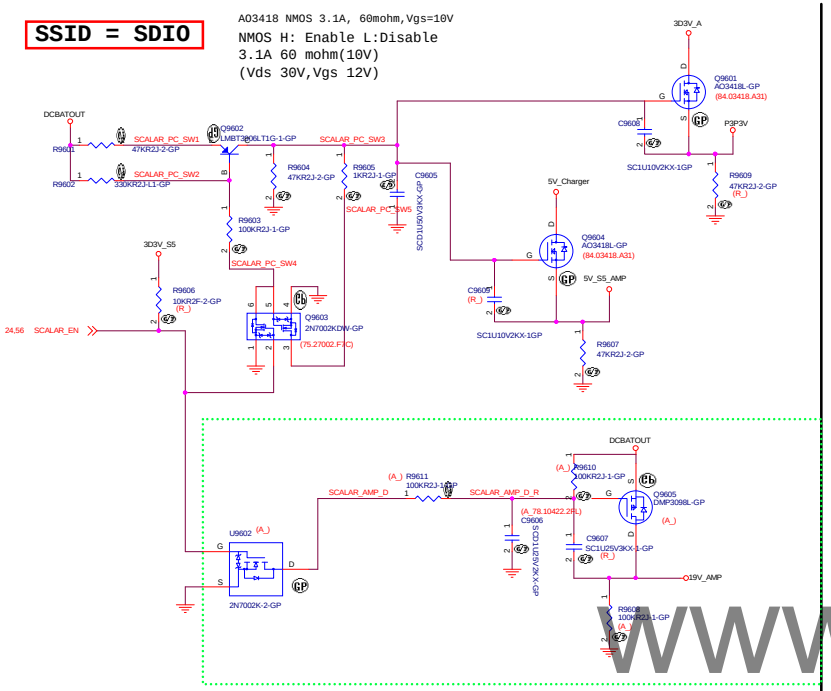
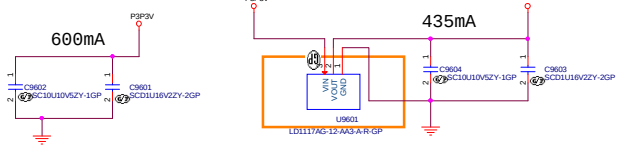
SSID = SDIO

AO3418 NMOS 3.1A, 60mohm,Vgs=10V
NMOS H: Enable L:Disable
3.1A 60 mohm(10V)
(Vds 30V,Vgs 12V)





Scalar Spec Table

GPI input		From	High	Low	Default
Pin69	GPI-1 PC Power ON → PM_SLP_S3# 20,24,34,40,41,49,50,95	SB	PC	Monitor	Monitor
Pin109	GPI-2 Mode change/ Panel OnOff	SW	Normal	Touch	PC: PC (PC->HDMI) Monitor: HDMI, VGA (HDMI)

GPO output

Pin55	GPO-2 Panel On/OFF → SCALAR_VDD_EN 55,95	Scalar	ON	OFF	PC: ON Monitor: Detect Signal
Pin104	GPO-3 PC/Monitor → PC_MONITOR_SW 28,95	Scalar	PC	Monitor	PC: PC, Monitor: HDMI, VGA
Pin101	GPO-5 Video → BLON_EN# 55,95	Scalar	Disable	Enable	Disable
	Delete AMP mute circuit, the mute function change to EC --Kai 0308				

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PCIE

18,31 PEG_CLK2_LAN
18,31 PEG_CLK2_LAN#
16,31 PCIE_TX_LAN_P5
16,31 PCIE_TX_LAN_N5
16,31 PCIE_RX_LAN_P5
16,31 PCIE_RX_LAN_N5

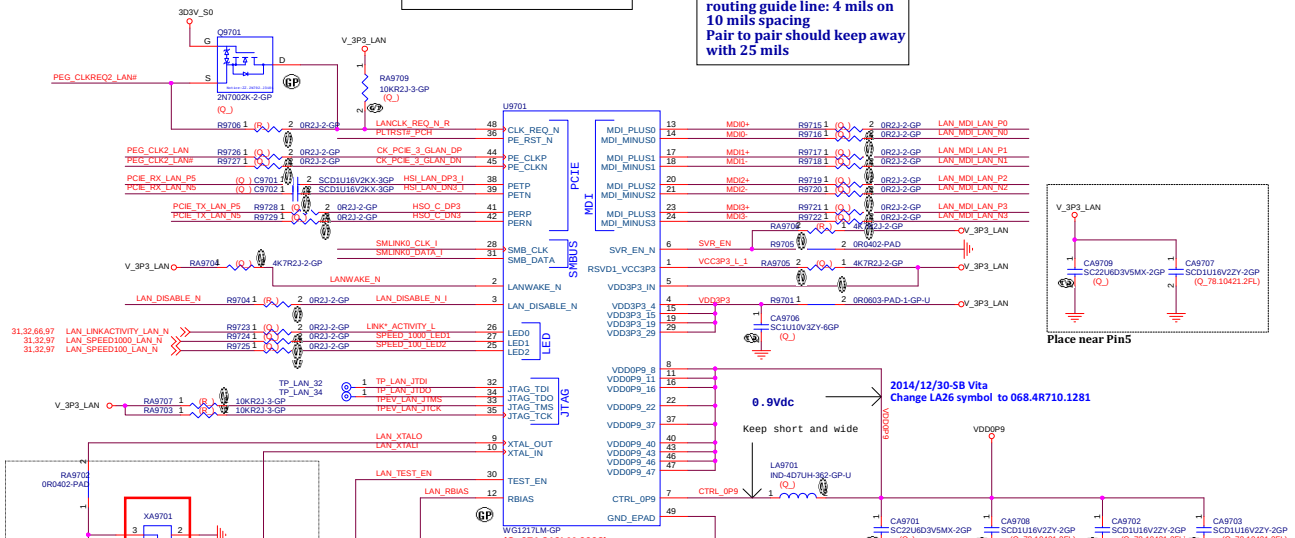
OTHERS

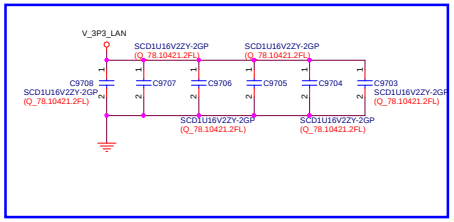
20 LAN_DISABLE_N
20 SMLINK0_CLK
20 SMLINK0_DATA
15,24,65,68,91 PLTRST#_PCH
24,31 LANWAKE_N
18,31 PEG_CLKREQ2_LAN#

31,32 LAN_MDI_LAN_P0
31,32 LAN_MDI_LAN_N0
31,32 LAN_MDI_LAN_P1
31,32 LAN_MDI_LAN_N1
31,32 LAN_MDI_LAN_P2
31,32 LAN_MDI_LAN_N2
31,32 LAN_MDI_LAN_P3
31,32 LAN_MDI_LAN_N3
31,32,97 LAN_SPEED1000_LAN_N
31,32,97 LAN_SPEED100_LAN_N
31,32,66,97 LAN_LINKACTIVITY_LAN_N
24,62 LAN_EN_PWR_SIO

If CLK_REQ_N is connected to PCIECLKRQ[1:2]#,the CLK_REQ_N pull-up resistor should be connected to +V3.3S.

LAN_MDI_P / LAN_MDI_N routing guide line: 4 mils on 10 mils spacing
Pair to pair should keep away with 25 mils





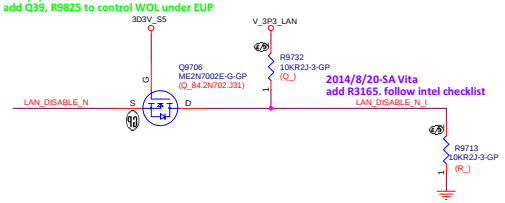
10Mb: Green
100Mb: Green
1Gb: Orange
Active: Yellow Light flash

0.9Vdc POWER OPTIONS

Internal SRV	Shared with PCH's 1.05V SVR
LA36 : STUFF	LA36 : NO STUFF
RA1020 : NO STUFF	RA1020 : STUFF
R968 : STUFF	R968 : NO STUFF
RA886 : NO STUFF	RA886 : STUFF

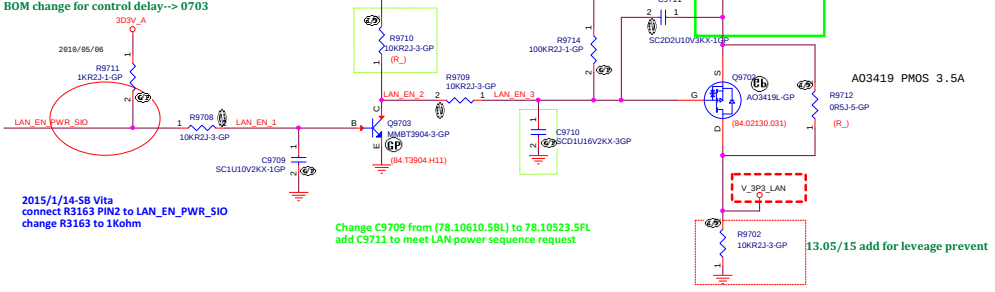
*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply (example sharing from PCH's 1.05V SVR). When sharing, make sure the 1.05V_SHARED is controlled by the SLP_LAN signal. Both +3.3V_LAN and 1.05V_SHARED rails are remained powered on during ALL Sx states, as required to support WOL.

2015/3/19-1A Vita
add Q39, R9825 to control WOL under EUP

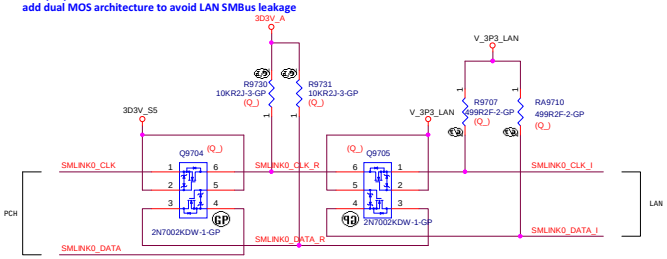


LAN Power

Mount LAN PWR delay circuit --> Verify SA
BOM change for control delay--> 0703



2014/12/31-SB Vita
add dual MOS architecture to avoid LAN SMBus leakage



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Title: Inter LAN
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Rev: SA
Date: Thursday, November 26, 2015
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2015/11/18 Rossi
Remove XDP connector

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Title
XDP&ITP

Size	Document Number	Rev
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Title
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Title: GPIO table

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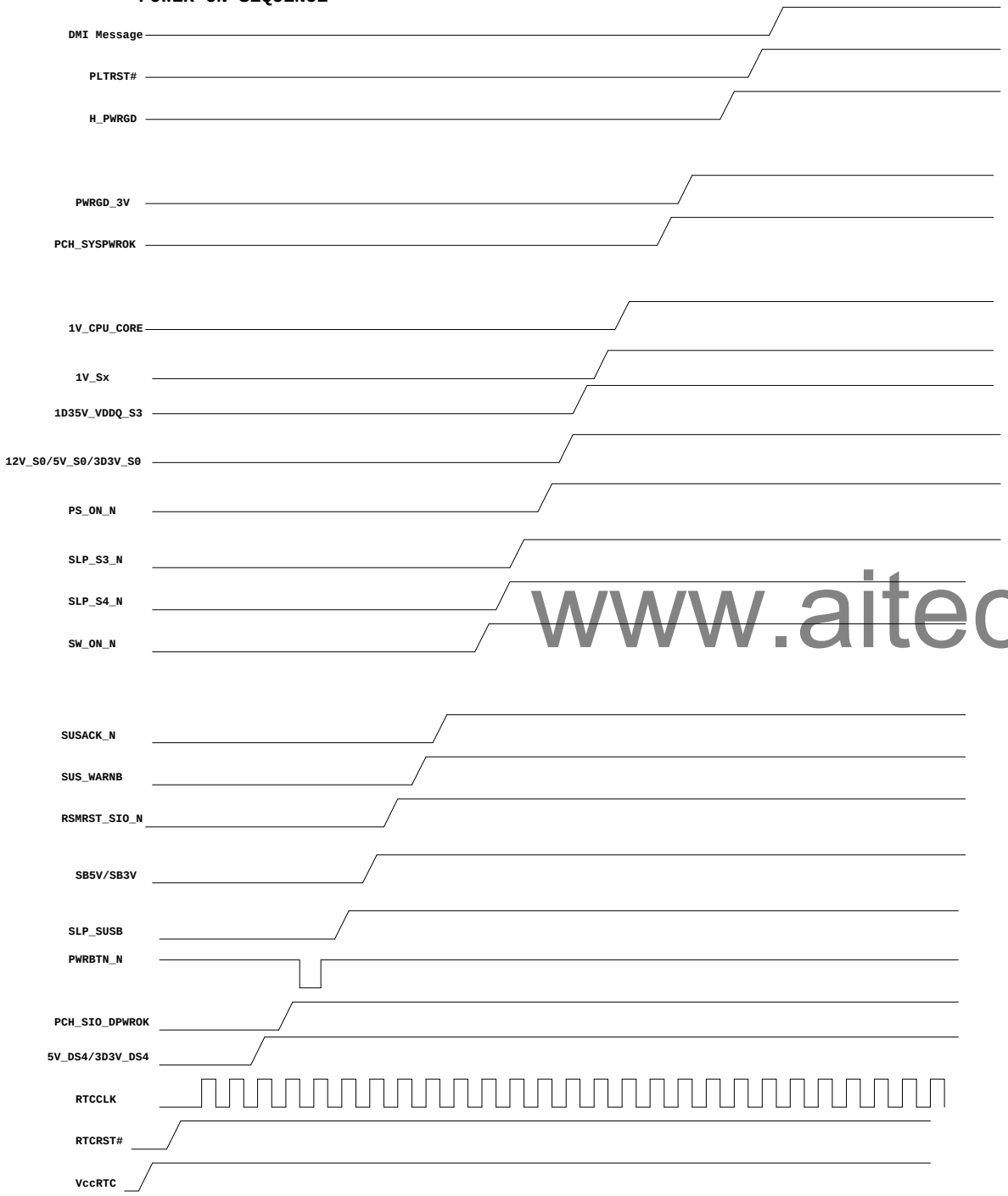
POWER ON SEQUENCE



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Title: Power sequence

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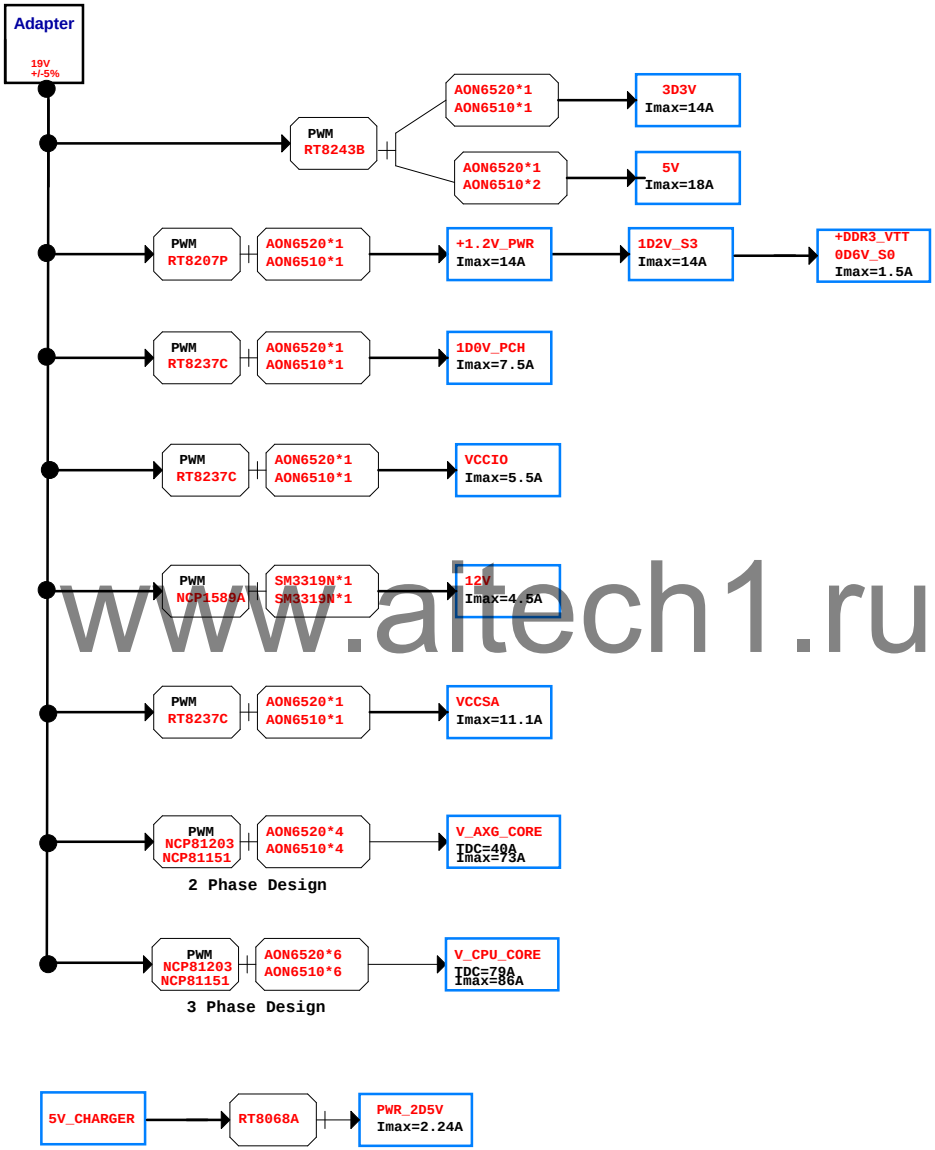

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Title: Power Block Diagram

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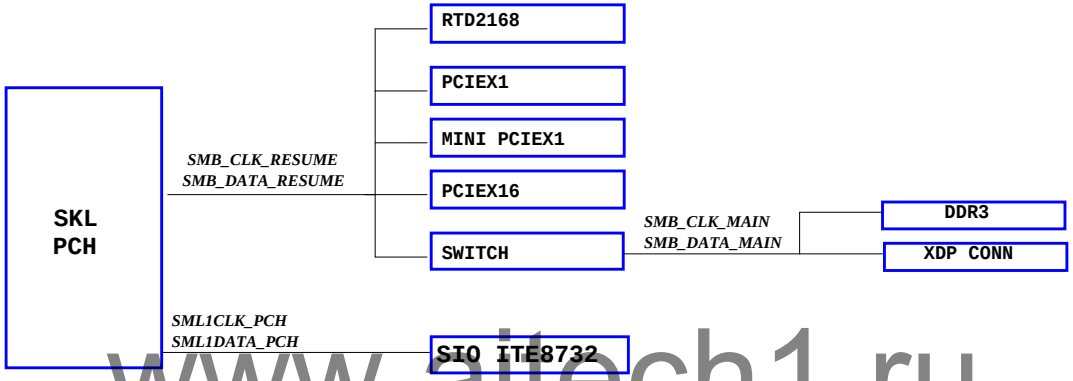

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Title: SMBUS Block Diagram

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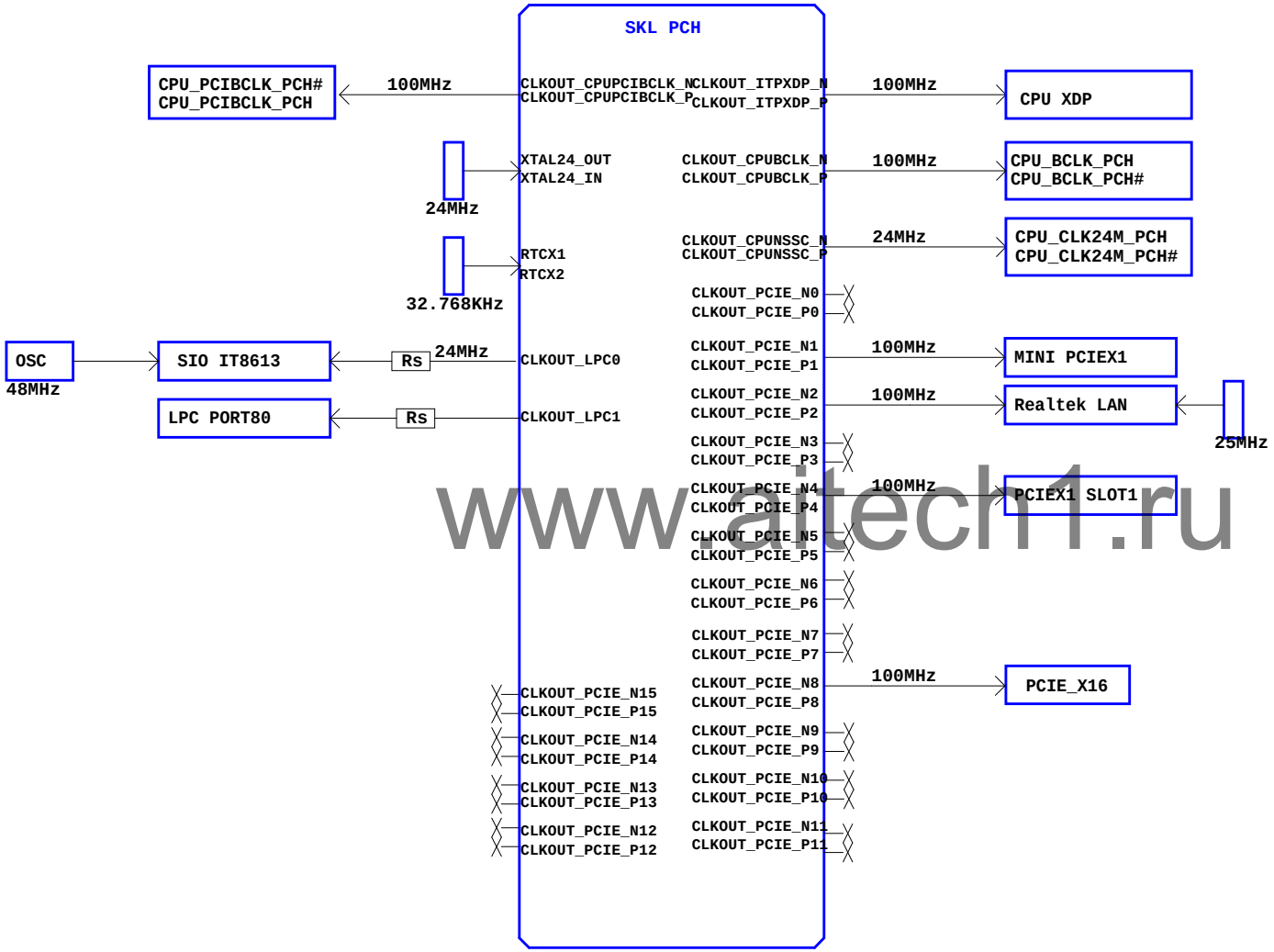

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Title: Clock MAP

Size: C | Document Number: Consumer AIO Woody | Rev: SA

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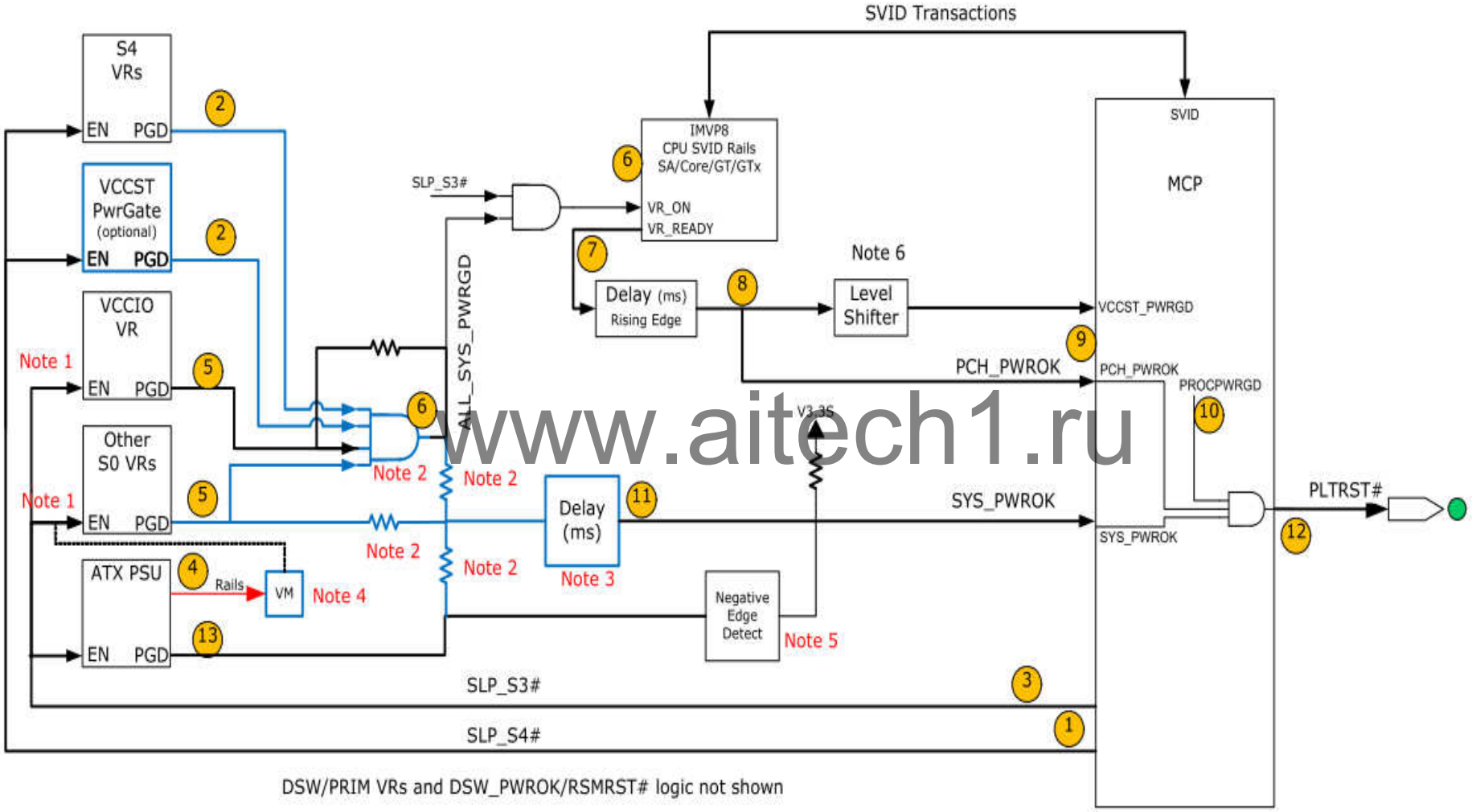

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Title: RESET Flow Chart

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Title: Change History

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